Front-End Technologies for nano-scale MOSFETs

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1. Introduction

We are working for development of front-end process and device technologies of nano-scale MOSFETs. Our COE project aims development of 3DCSS system. High-performance mixed-signal device technologies are demanded for such a system. The major our research targets are shallow junction formation and metal-gate workfunction tuning. These are standard development for CMOS logic application., in addition, helpful for improvement of RF device performance. Low resistive shallow junction formation is indispensable to improve f_T that is degraded by parasitic series resistance. Gate resistance reduction by replacing poly-Si gate with metal gate is effective for f_{MAX} improvement. In this abstract, these research activities are briefly introduced.

2. Metalgate tecnology

The most fundamental motivation for development of metal gate MOSFETs is solving the gate depletion problem. The gate depletion is unavoidable for a poly-Si gate structure and is the origin of penalty for effective gate oxide thickness. By replacing semiconductor, that is poly-Si, with metal the gate depletion problem can be removed. However, it also means losing the benefit of workfucntion tuning by doping. A dual gate structure that utilizes high and low workfunction for p- and n-MOS threshold voltage adjustment and that is indispensable for CMOS devices (Fig. 1). Therefore, one of the most important development target of metalgate is metal workfucntion tuning technology.

We have working on workfunction tuning of Mo and silicides. As shown in Fig.2, metal workfunction of a Mo MOS structure can be varied by nitrogen pileup formation at Mo/SiO_2 interface [1,2]. Electric dipole formed by high concentration impurity at the metal/insulator interface (Fig.3) is considered to be origin of the workfunction shift [3,4]. We have fabricated MOSFETs with the Mo gate and found nitrogen redistribution during additional thermal treatment process for FET fabrication [5,6]. Thus, metalgate workfunction tuning technology must be confirmed through integration to the device fabrication.

Fully silicided (FUSI) gate is also another candidate for workfunction tunable metalgate. Though combination of ploy-Si gate and silicide is already integrated into commercially available devices as polycide gate or salicide gate, FUSI dose not remain poly-Si by reaction process of poly-Si and metal deposited on the poly-Si. Workfunction of a FUSI MOS structure is also tunable by pileup formation of impurities at the interface of silicide and SiO_2. We have investigated the relationship between silicidation condition of NiSi FUSI gate and its workfunction [7,8]. NiSi is the most popular material for the FUSI gate. Details of obtained results are shown in another paper of this workshop [9]. We are also working on Pd_2Si as an alternative candidate of FUSI gate material [10].

3. Shallow Jucntion formation by laser annealing

Currently RTP based annealing technologies are used for source and drain (S/D) formation of leading edge device mass production. New annealing technologies that is suitable for shallower S/D are demanded for further scaling of CMOS devices. Melt laser annealing (LA) is one of such technologies. Though LA has long development history, melt LA currently stands for LA that utilizes melting point difference between crystalline Si and amorphous Si. Selective melting of a thin amorphous Si layer that has lower melting point prevents over-melt to crystalline Si and leads to high activation due to non-equilibrium re-crystallization. Amorphous layer can be formed heavy ion, such as Ge^+, implantation prior to dopant implantation.

We used two laser source shown in Fig. 4. One is KrF excimer laser and another is all-solid-state green laser. Both lasers provides nanosecond order pulse. We have proposed the combination of substrate heating and LA, that is heat-assisted LA (HALA) [11-13]. This method was applicable to ultra-shallow junctions shallower than 20 nm and sheet resistance lower than 1 kΩ/sq. was easily obtained. Based on heat-assisted LA, we have proposed a new LA scheme, partial-melt LA (PMLA). This scheme utilizes solid-phase regrowth of amorphous-Si during preparation heating for HALA. By stopping appropriate timing, amorphous layer thinner than initial thickness can be obtained. This provides separation of juncntion depth and amorphous layer thickness, which means increase in process design freedom. We have demonstrated PMLA with 10 nm junction formation [14,15]. Sheet resistance about 700Ω/sq. was obtained for 10 nm junctions with negligible diffusion, as shown in Fig. 6. Green laser has deep penetration depth compared with KrF excimer laser. This leads to increase in laser power, in other words difficulties for development of production equipments. To compensate this problem, we are working on green laser annealing with light absorber. We have discussed selection of light absorber materials and their layered structures based on both experimental and simulation results [16-19].

4. Summary

Our activities on front-end device fabrication technologies beneficial for mixed-signal application like 3D-CSS was introduced. We are currently working integration of these technologies for MOSFET fabrication to demonstrate their usefulness.

Acknowledgements

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1. T. Amada et al., MRS Proc., **716** (2002) p. 299.
2. K. Shibahara, Abst. of 1st. Hiroshima Int. Workshop on NTIP, 2003, p. 38.

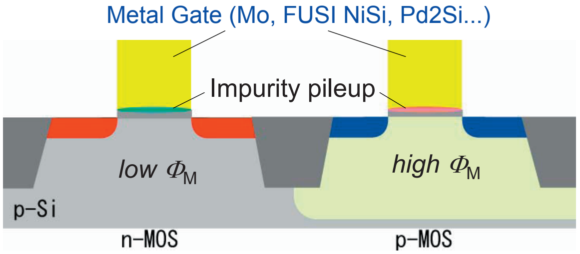

Fig. 1 Schematic model of ingle-metal dual-workfunction CMOS. By forming impurity pileup at the metal/gate insulator interface, metal workfucntion can be tuned.

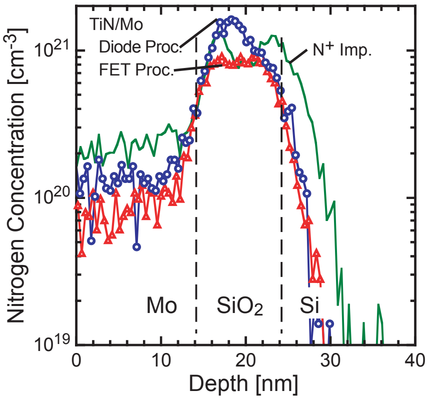

Fig. 2 Nitrogen back-side SIMS profiles in a Mo/SiO_2/Si MOS structure. Nitrogen pileup was formed after adequate annealing.

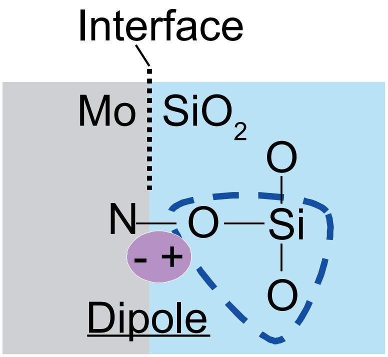

Fig. 3 A model to explain Mo workfunction shift. By the difference of electron negativity, electric diopoles are formed at the Mo/SiO_2 interface.

3. M. Hino et al., Ext. Abst. SSDM 2003, p.494.
4. K. Sano et al., Abst. of 2nd. Hiroshima Int. Workshop on NTIP, 2004, p. 58.
5. T. Hosoi et al., Abst. of MRS 2005 spring meeting, pp.191-192.
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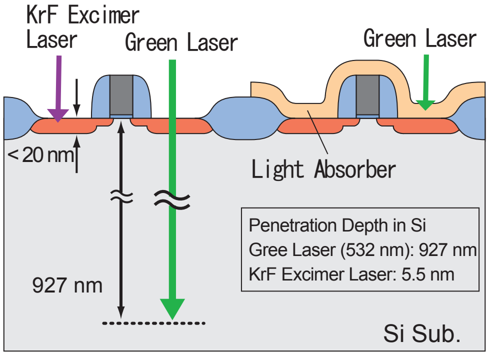

Fig. 4 Penetration depth of KrF excimer laser and green laser light.

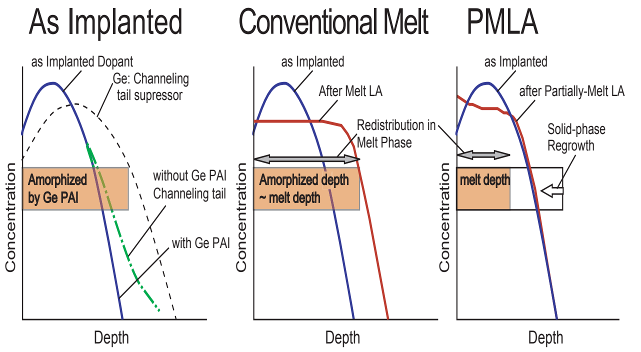

Fig. 5 Relationships between dopant profiles and amorphized layer depth before and after melt laser annealing.

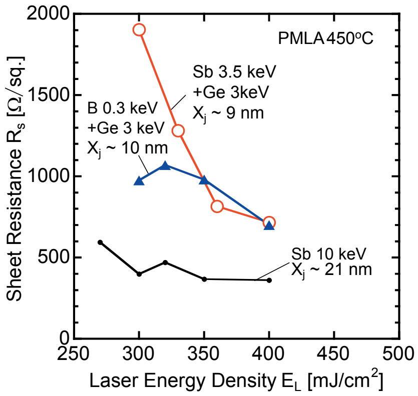

Fig. 6 Sheet resistance of ultra-shallow jucntions formed with PMLA.

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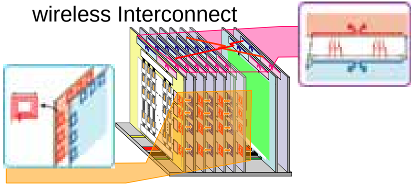
Fundamental Device Technologies for 3DCSS

3DCSS System

multi-chip information processing with wireless Interconnect



Tera-bit processing → high RF performance devices

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

Parasitic series resistance should be low
→ Low resistive junction formation
→ Laser Annealing

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{gd} R_g}}$$

Gate resistance should be low
→ Metal gate

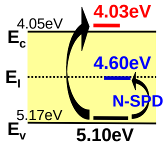
Workfunction Tunable Metal Gate

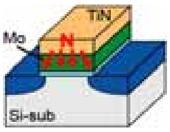
- ◆Mo gate with Nitrogen pileup formation: This poster
- ◆NiSi FUSI: visit poster P-26
- ◆Pd_2Si FUSI: coming next time

Mo Gate Workfunction Tuning by Nitrogen-Dope

- Nitrogen ion implantation
  - sufficient workfunction shift, $\Delta\Phi_{Mo}$ = -1 eV
    (P. Ranade et al., MRS2000, **611**, C.3.2.1)

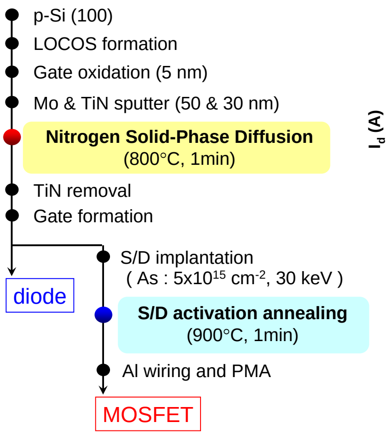
  but…
  - increases in interface state & leakage current
    (T. Amada et al., MRS2002, **716**, 299)
- **Nitrogen solid-phase diffusion (N-SPD)**
  - $\Delta\Phi_{Mo}$ = -0.5 eV
  - No degradation
    (R.J.P. Lander et al., MRS2002, **716**, 253)
    (M. Hino et al., SSDM2003, 494)



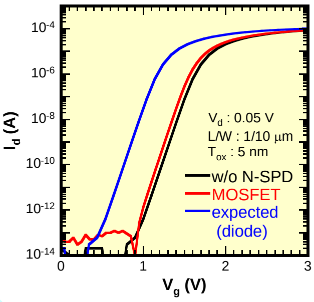


⇨ Fabrication of Mo Gate MOSFET with N-SPD

Nitrogen Solid-Phase Diffusion into Mo Gate



- p-Si (100)
- LOCOS formation
- Gate oxidation (5 nm)
- Mo & TiN sputter (50 & 30 nm)
- **Nitrogen Solid-Phase Diffusion** (800°C, 1min)
- TiN removal
- Gate formation
  - diode
  - S/D implantation (As : 5x10^{15} cm^{-2}, 30 keV)
  - **S/D activation annealing** (900°C, 1min)
  - Al wiring and PMA
  - MOSFET

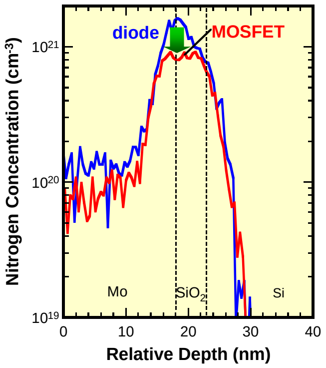


	$\Delta\Phi_{Mo}$
diode	-0.46 eV
MOSFET	-0.1 eV

M.Hino et al., SSDM2003, 494.

Nitrogen Redistribution by S/D Activation Annealing

back-side SIMS



Mo-gate MOSFET

Reduction of N concentration at Mo/SiO_2 interface (N out-diffusion)

⬇

Reversible workfunction shift

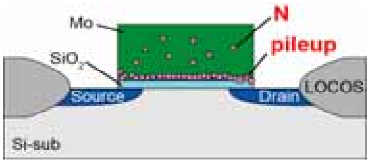
(-0.46 eV → -0.1 eV)

Modification in fabrication process

Nitrogen Redistribution in Mo Gate (Oxide-cover)

just after N-SPD

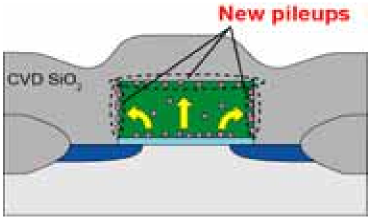
N pileup at Mo/SiO$_2$ interface was formed



after S/D activation annealing

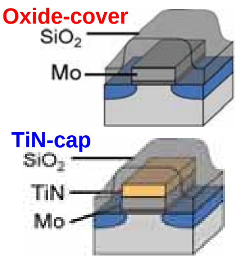
<u>N pileup at bottom Mo/SiO$_2$ Interface redistributes toward top and two side interfaces.</u>

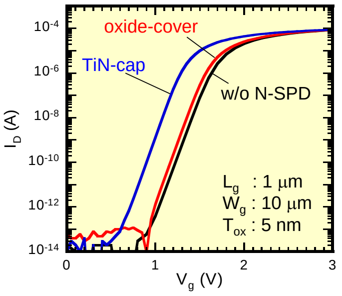
small V$_{th}$ shift



Device Characteristics of Oxide-cover & TiN-cap

Modified Device Structures





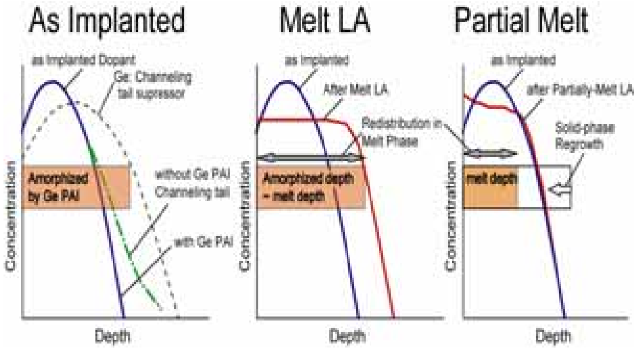
Oxide-cover : ΔV_{th} = -0.1 eV
- <u>same as standard process</u>

TiN-cap : ΔV_{th} = -0.33 eV
- enlarge V$_{th}$ shift (still smaller than MOS diode case)

Ultra Shallow Junction Formation

- ◆Proposal of New Scheme
  - ◆Pre-amorphization Implantation
  - ◆Solid Phase Regrowth
  - ◆Laser Irradiation
    - ◆Partial Melt Laser Annealing

Basic Ideas of Schemes

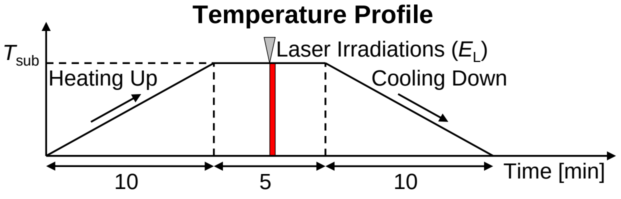


PMLA: melt(Good activation) + non-melt(Diffusion less)

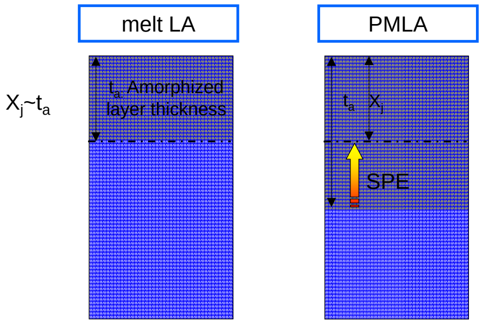
PMLA Time Sequence

Substrate Temperature (T_{sub}): **250 – 525°C**
- Laser Energy Density (E_L) : **200 – 600 mJ/cm^2**
- FWHM of Laser Pulse: 38 ns, Pulse Number: 1 Pulse

Temperature Profile

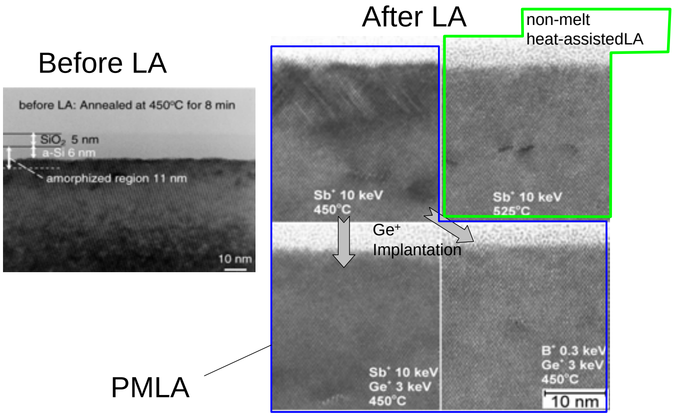


Advantage of PMLA

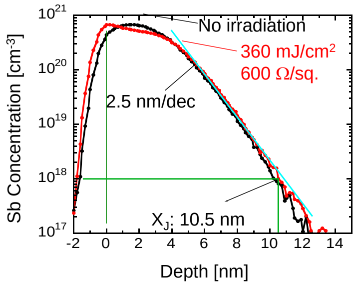


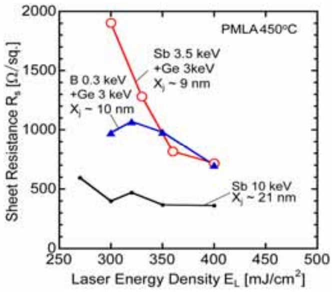
PMLA:
Amorphization depth is free from junction depth

XTEM before and After Laser Irradiation

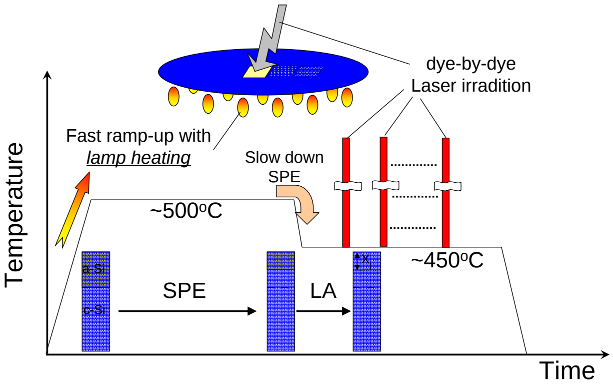


10 nm Junction Formation with Sb and B





Improved Sequence of PMLA



For more details: Publication List

Mo gates

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2. K. Shibahara, Abst. of 1st. Hiroshima Int. Workshop on NTIP, 2003, p. 38.
3. M. Hino et al., Ext. Abst. SSDM 2003, p.494.
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NiSi FUSI

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PMLA

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Green Laser Annealing with Light Absorber

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