Workfunction Tuning of Fully-Silicided NiSi Gate with Poly-Si Predoping

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1. Introduction

Metal gates are expected to replace conventional poly-Si gate in order to eliminate a depletion effect and boron penetration. Since single gate material with dual-workfunction is required for the existing CMOS fabrication process, workfunction tuning technique for several metals has been extensively investigated. Recently, fully-silicided (FUSI) metal gates have been demonstrated based on the extension of self-aligned silicide (SALICIDE) technology. The workfunction of FUSI NiSi gate can be tuned by impurity pileup formed at $NiSi/SiO_2$ interface [1-5]. Furthermore, the workfunction of Ni silicide ($NiSi_x$) depends on the composition ratio of Ni/Si [6]. However, the workfunction tunable range of FUSI $NiSi_x$ is still insufficient for high performance CMOS devices. Furthermore, Ni silicide phase difference between long- and short-channel FETs should be addressed [7]. Issues such as voiding [4, 8] and a-Si formation [9] were also found in FUSI gate structure. Therefore, it is important to establish the FUSI process taking into account the controllability of silicide formation. In this paper, not only the workfunction shift in FUSI NiSi gate with poly-Si predoping but also side effects such as the void formation at $NiSi/SiO_2$ interface and controllability of silicide phase formation are discussed.

2. Experiment

Figure 1 shows the FUSI NiSi gate MOS diode fabrication process flow. The poly-Si predoping conditions (implantation species, dose, and energy) are listed in Table I. Silicidation was carried out at 400 °C, 450 °C, or 500 °C by in-situ lamp heating in a vacuum just after Ni deposition. Although Ni-rich phase (Ni_2Si) is found at the initial stage of silicidation, transformation to Ni monosilicide phase (NiSi) is completed after prolonged anneals, as shown in Fig. 2. NiSi gate workfunction is extracted from C-V characteristics of MOS diodes with area of 10^{-4} cm^2. As shown in Fig.3, the workfunction of undoped NiSi gate is determined to be 4.63 eV.

3. Results and Discussion

Table I shows a summary of flatband voltage (V_{FB}) shift for various impurity species [10]. It is noteworthy that Ge, which is not a dopant for Si, caused the V_{FB} shift. Figure 4 shows the C-V characteristics of Ge predoped NiSi gate MOS diodes with two different implantation doses. The V_{FB} shift increases with implantation dose. The Ge depth profile in NiSi MOS structure measured by back-side SIMS confirms that Ge concentration at the oxide interface and in NiSi film is dependent on the implantation dose. In the case of Sb predoped NiSi MOS diodes, silicidation at the 500 °C resulted in a small V_{FB} shift, but the larger V_{FB} shift (-0.34 eV) was obtained for lower silicidation temperature (Fig. 5). This difference also originates from the Sb concentration at $NiSi/SiO_2$ interface. On the other hand, it should be noted that reduction in the accumulation capacitance was observed for 400 °C and 450 °C. In addition, partial NiSi film peeling was found after unreacted Ni removal with acid only for silicidation temperature below 450 °C [8]. This is attributed to void formation at the $NiSi/SiO_2$ interface.

The similar side effect was also observed for In predoped sample. As shown in Fig. 6(a), reduction in accumulation capacitance in C-V characteristics and the V_{FB} shift were observed. We speculated that In driven to the oxide interface formed a interfacial layer by the reaction with the oxide, which leads to charge formation and increase in insulator thickness. To judge accuracy of this speculation, SiN was deposited on the oxide film to prevent the interfacial reaction. As a result, though V_{FB} shift decreased, accumulation capacitance reduction still remained as shown in Fig. 6(b). Cross-sectional observation by SEM in Fig. 7 revealed that the capacitance reduction is attributed to void formation at the interface. Although the void formation mechanism is not clear yet, it is assured that impurity concentration in the vicinity of the interface is the key factor. This voiding should be noted as a potential roadblock against practical use of fully silicided NiSi gate.

5. Conclusion

Full silicidation of NiSi gate with poly-Si predoping for workfunction tuning was investigated. It was found that Ge that is not a dopant for Si causes the workfunction shift depending on the doping concentration. On the other hand, there still exist some problems such as the void formation and the interfacial reaction at the $NiSi/SiO_2$ interface. Previous works on FUSI NiSi gate have been mainly focused on workfunction tuning [1, 3], but recently Kittl *et al.* have addressed Ni silicide phase control in FUSI process in terms of the device scalability [7]. Thus, a fundamental understanding of the kinetics of silicide formation is essential for practical application,

Acknowledgements

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References

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- p-Si (100)
- LOCOS formation
- Gate oxidation(10 nm)
- poly-Si deposition(100 nm)
- **Impurity Ion Implantation**
  (N, F, B, P, Sb, Ge, In)
- Ni deposition(60 nm)
- **NiSi Full-Silicidation**
  (400, 450, 500 °C)
- Unreacted Ni removal
- Post metallization annealing

Fig. 1 Fabrication process flow of fully silicided NiSi gate MOS diodes.

Table I Impurity implantation conditions and resulting V_{FB} shift. Standard silicidation temperature was 500 °C.

	Dose(cm^{-2})	Energy(KeV)	ΔV_{FB} (V)
N	5.0 x 10^{15}	10	~ 0
F	2.5 x 10^{15}	10	~ 0
B	1.0 x 10^{15}	5	> 0
P	5.0 x 10^{15}	15	< 0
Sb	5.0 x 10^{15}	30	< 0
Ge	5.0 x 10^{15}	30	< 0
In	5.0 x 10^{15}	30	< 0 ?

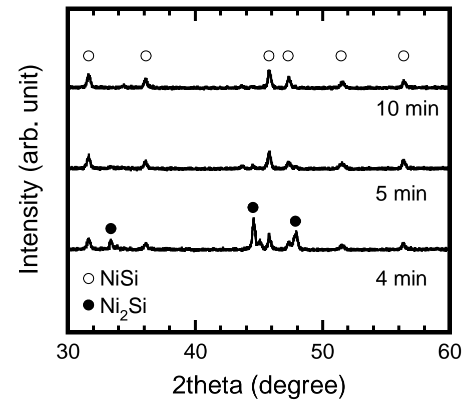

Fig. 2 XRD spectra of NiSi MOS structure with various silicidation time at 500 °C.

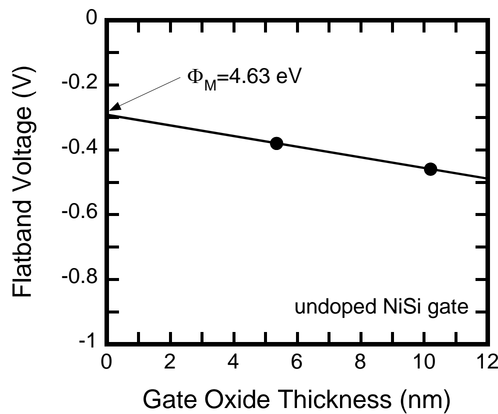

Fig. 3 Flatband voltage of undoped FUSI NiSi gate MOS iodes extracted from the C-V characteristics as a function of gate oxide thickness.

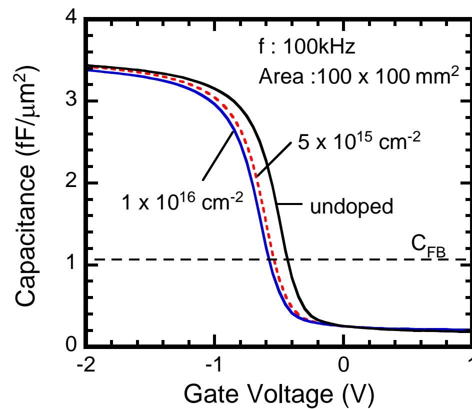

Fig. 4 C-V characteristics of Ge predoped NiSi gate MOS diodes.

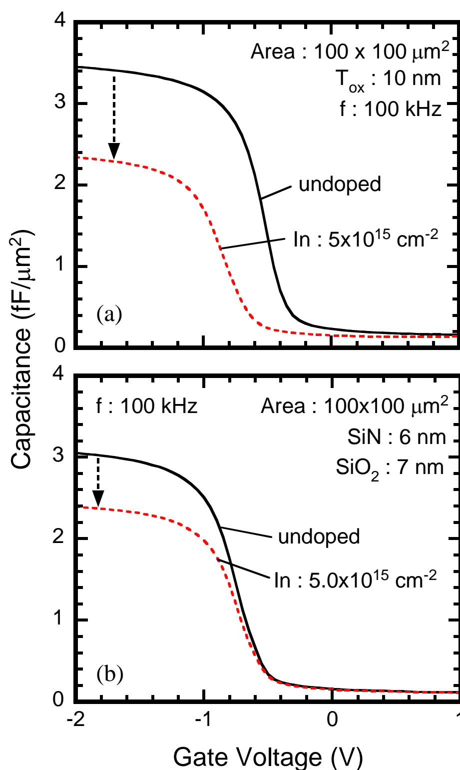

Fig. 6 C-V characteristics of Sb predoped NiSi gate diodes. Gate insulators are SiO_2 (a) and SiN/SiO_2 stack (b).

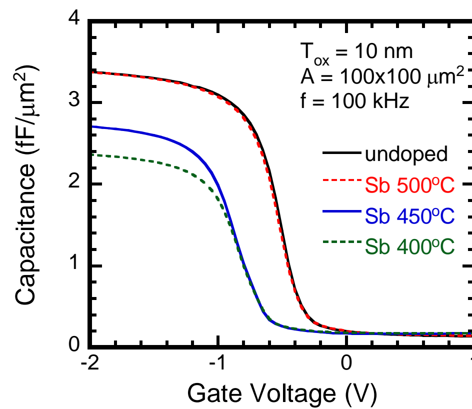

Fig. 5 C-V characteristics of Sb predoped NiSi gate MOS diodes.

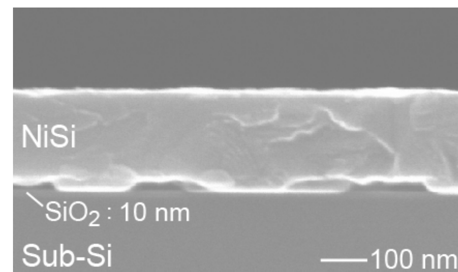

Fig. 7 Cross sectional SEM micrograph of In predoped NiSi/SiO2/Si interface. Voids at the NiSi/SiO2 interface were found.

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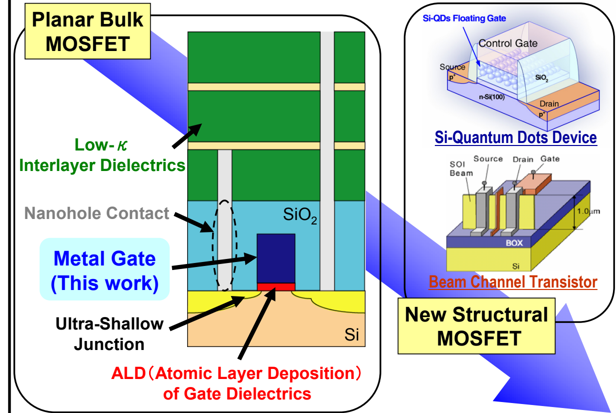
Fundamental Device Technology in 21st COE Program



Why Metal Gate ?

■ Merit & Task of Metal Gate

Merit : ◎ Elimination of poly-Si depletion effect
→ Thinning of EOT

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_g - V_{th})^2$$

◎ No boron penetration
◎ Mobility enhancement (S. Datta *et al.*, IEDM2003)

Task : ▼ CMOS process compatibility
▼ Dual workfunction for p-/n-MOSFET
(pFET : 5.17eV, nFET : 4.05 eV)

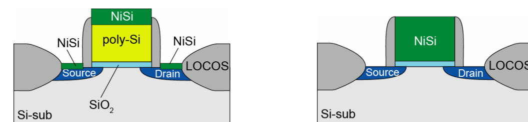
■ Metal Candidate

TiN, TaN, FUSI, W, ･･･etc
Fully-Silicided gate (NiSi, PtSi,…)

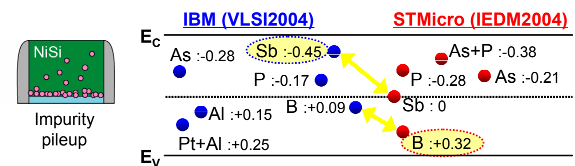
Fully-Silicided (FUSI) NiSi Gate

poly-Si gate
+ Self-aligned Silicide (SALICIDE)

FUSI NiSi gate

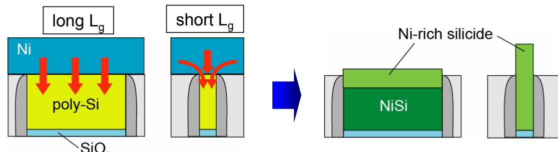


■ Workfunction of NiSi : 4.6 - 4.7 eV (W.P.Maszara *et al.*, IEDM2002)
※ Tunable with poly-Si predoping (J.Kedzierski *et al.*, IEDM2002&2003)



Issues of FUSI NiSi Gate

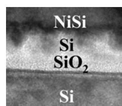
■ Control of $NiSi_x$ phase for scaled devices (J.A. Kittl *et al.*, VLSI2005)



■ $NiSi/SiO_2$ interface

D. Aimé *et al.*, IEDM2004

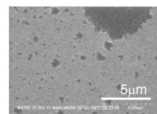
As predoped



Remaining amorphous Si

K.Sano et al., SSDM2004

Sb predoped

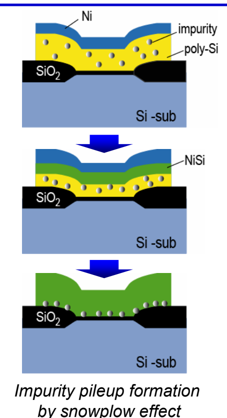


NiSi peeling off due to void

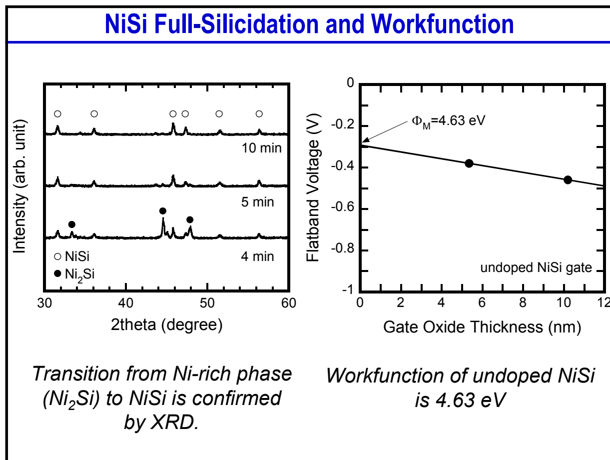
Objective : Investigation of NiSi formation focusing on interface

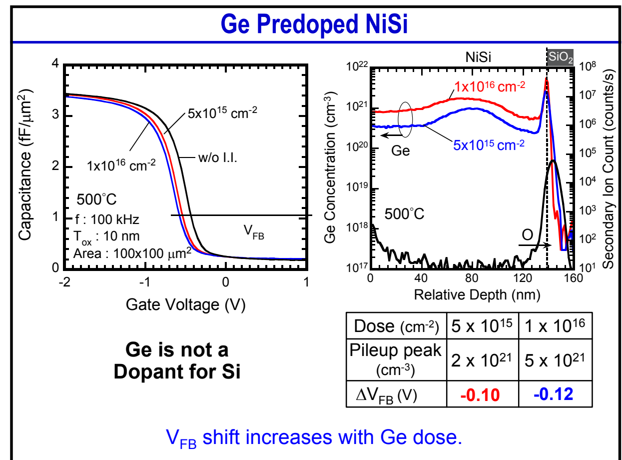
Fabrication Process of FUSI NiSi Gate MOS Diodes

- p-Si (100)
- LOCOS formation
- Gate oxidation (10 nm)
- Poly-Si deposition (100 nm)
- Impurity Ion Implantation (Sb, Ge, In)
- Ni sputter deposition (60 nm)
- NiSi Full-Silicidation (400°C, 450°C, 500°C)
- Unreacted Ni removal ($H_2SO_4 + H_2O_2$)
- Post metallization annealing (400°C, in $H_2 + N_2$)

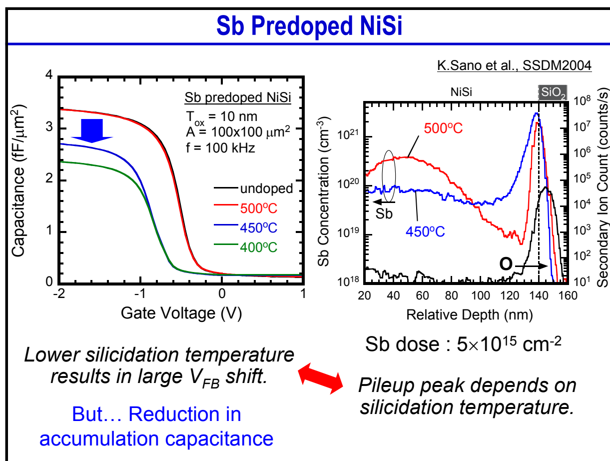


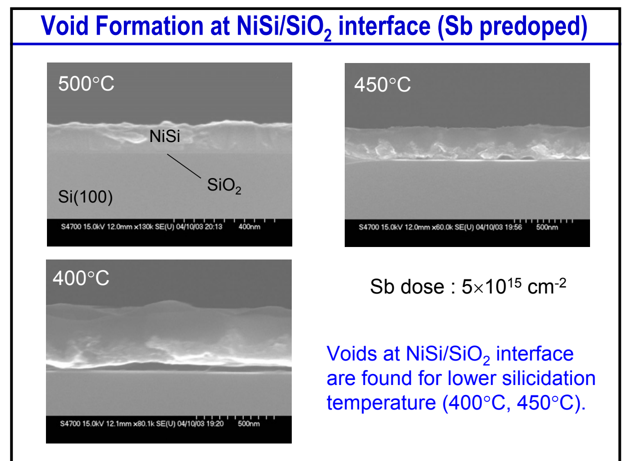
Impurity pileup formation by snowplow effect

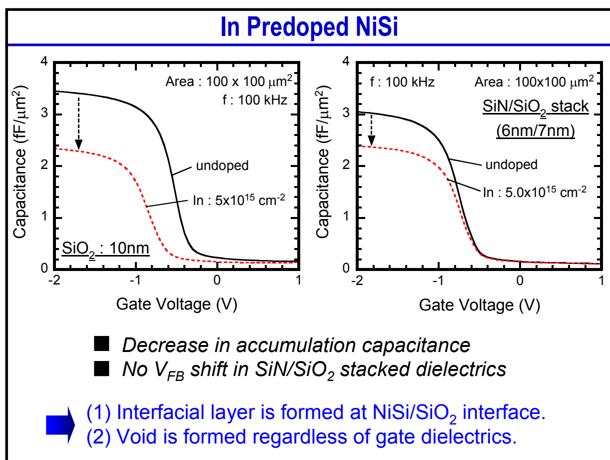




Dose (cm-2)	5 x 10^15	1 x 10^16
Pileup peak (cm-3)	2 x 10^21	5 x 10^21
ΔVFB (V)	-0.10	-0.12







Conclusion

FUSI NiSi gate with poly-Si predoping was investigated.

- Ge predoping causes workfunction shift depending on dose.

  Possibility of other impurities

- Some issues remain in FUSI NiSi gate.
  - Void & interfacial layer formation at $NiSi/SiO_2$ interface
  - Ni-silicide phase control for scaled devices

(J.A. Kittl *et al.*, VLSI2005)

Need to understand the fundamental kinetics of Ni-silicide formation

Acknowledgement

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