Development of Three-Dimensional Beam-Channel MOS Transistors

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1. Introduction

To realize various functionalities of LSI's, different kinds of devices have been required to be monolithically integrated in an LSI chip. One example is power transistor which is connected in series to a circuit block providing ultra-low stand-by current by switching the pull-down power transistor, as schematically shown in Fig. 1.

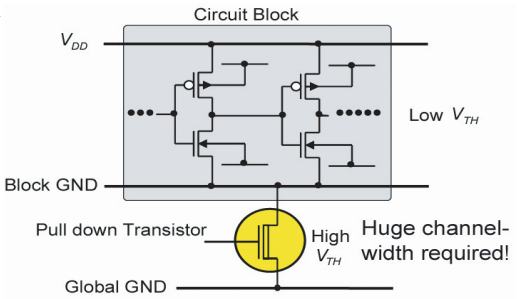

Fig. 1 An application of on-chip power transistor for ultra-low stand-by power circuit.

To make the transistor as small as possible, corrugated-channel transistor, CCT [1] has been proposed, as shown in Fig. 2. The CCT is a type of BCT with plural channels. The folded channel provides reduced planar area. Targets of the BCT are shown in Fig. 3 as compared with conventional FINFET [2].

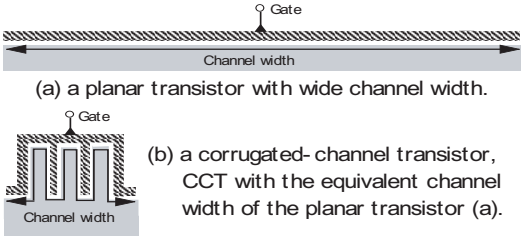

Fig. 2 Cross section of corrugated-channel transistor, CCT (b) of which channel width is equivalent to that of planar transistor.

2. Experimental and Discussion

Key techniques to realize the BCT are (a) high-aspect ratio lithography and etching, (b) three-dimensional (3-D) gate formation, (c) 3-D impurity doping, and (d) conformal electrode formation [3]. Electron beam exposure system is employed to delineate up to 2-μm thick photoresist. Orientation-dependent preferential etching with tetra-methyl-ammonium-hydroxide, TMAH is used to form silicon beams on (110) substrate.

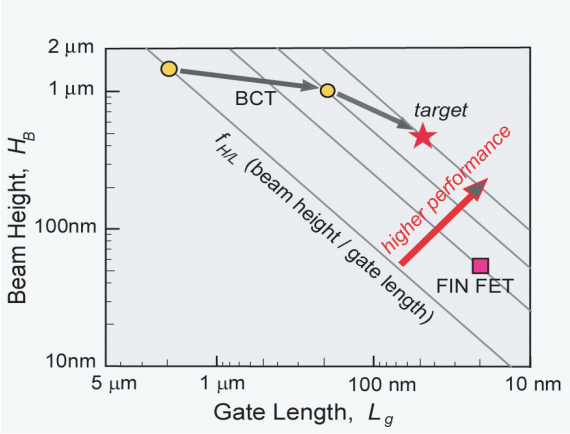

Fig. 3 Targets of the BCT in terms of planar area-normalized current drivability.

A realized structure having 31 silicon beams is shown in Fig. 4. Conformal gate delineation on tall silicon beam is also a key to realize sub-μm gate length however, there may be no choice but to utilize isotropic etching at present. Less-directional plasma etching technique can realize the gate length almost equal to the height of the silicon beam at present.

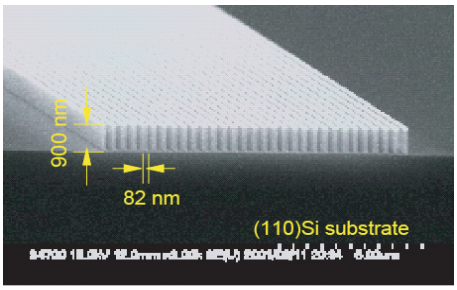

Fig. 4 An SEM cross section of channel of the target A of BCT, etched with TMAH, having 31 silicon beams on (110) surface.

Since strongly directional ion implantation may not be adequate to achieve uniform doping to tall comb-shaped silicon beams, plasma doping with AsH_3+Ar is utilized to form lightly-doped region along the beam surface. Figure 5 shows a cross section of a silicon beam which is doped with this plasma doping. It is evaluated that the beam is uniformly doped even in the bottom region of the beam. An obtained typical sheet resistance value is about 500 Ω/sq. This is adequate for the extension doping.

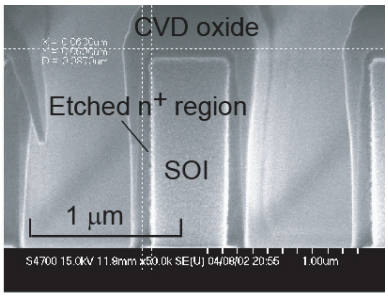

Fig. 5 An SEM cross section of AsH_3 plasma-doped region along beam surface.

Very low resistance of source and drain (S/D) regions are also inevitable not to sacrifice transistor drivability. Ni-silicided S/D achieves resistivity of 2.5×10^{-5} Ω-cm. A cross section of Ni-silicide beam is shown in Fi.g 6. The resistivity of the silicided beam is about 20-times lower than that of heavily doped n^+ silicon.

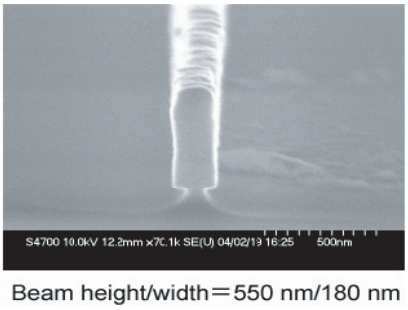

Fig. 6 An SEM cross section of Ni-silicide silicon beam.

Obtained drain currents are shown in Fig. 7 for the target A of the BCT of which channel structure is already shown in Fig. 4. Almost 5-times increase in the current is achieved as compared to the planar at the same planar area. A cross section and performance of the target B of BCT are shown in Figs. 8 and 9. Increased drain currents are realized in proportion to the number of the beams.

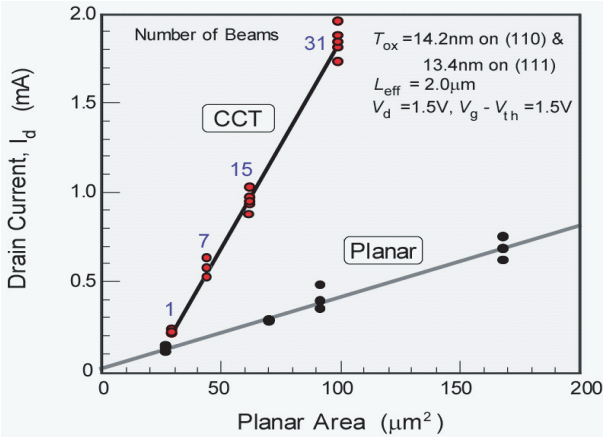

Fig. 7 Obtained drain current of the target A of BCT of which channel region is shown in Fig. 4.

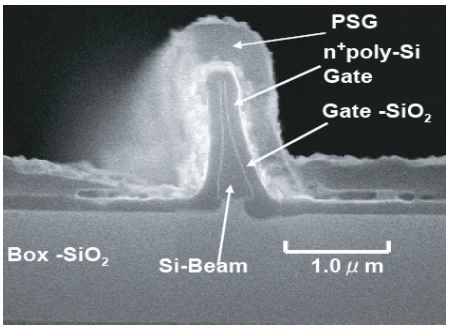

Fig. 8 An SEM cross section of the target B of BCT fabricated on (100) SOI substrate.

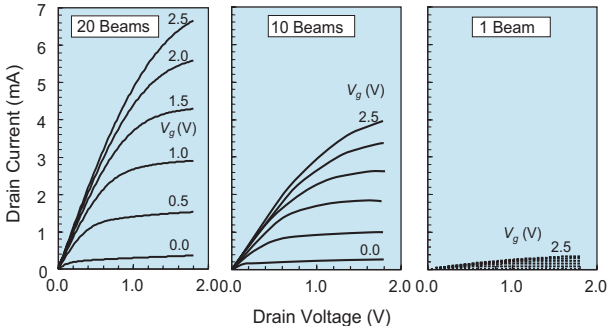

Fig. 9 Obtained drain currents of BCT of the target B fabricated on (100) SOI substrate.

3. Conclusion

Key techniques to realize 3-D MOS transistor such as the BCT are addressed. The BCT has strong potential for applying itself to area-conscious, i. e. cost-conscious LSI integrating on-chip power transistor. While, even if sub-half-μm gate length has already been obtained on 0.5-μm tall silicon beam, further scalability beyond sub-100 nm is not yet achieved.

Acknowledgements

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[1] T. Furukawa, H. Yamashita, and H. Sunami, Jpn. J. Appl. Phys. Vol.42, (2003) 2067-2072.
[2] Y-K. Cho, N. Lindert, P.Xuan, S.Tang, D. Ha, E. Anderson, T-J. King, J. Bokor, and C. Hu, IEDM Tech. Dig. Papers, (2001) 421-424.
[3] H. Sunami, T. Furukawa, and T. Masuda, Sensors and Actuators A 111 (2004) 310-316.

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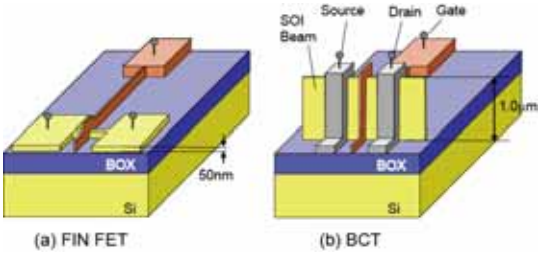
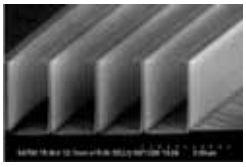
Research subjects of 3-D transistor

Research subjects associated with BCT

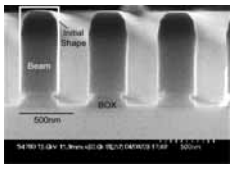
(A-1) Formation of tall Si beam
(A-2) Gate formation over tall Si beam
(A-3) Impurity doping for tall Si beam
(A-4) S/D contact over tall Si beam



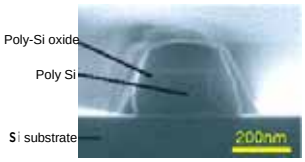
Results for each subject



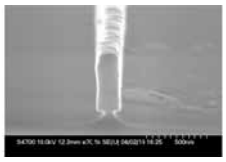
(A-1) 1.5-μm tall and 80-nm thick Si beams etched with by TMAH



(A-3) Uniform arsenic-doping by plasma doping.



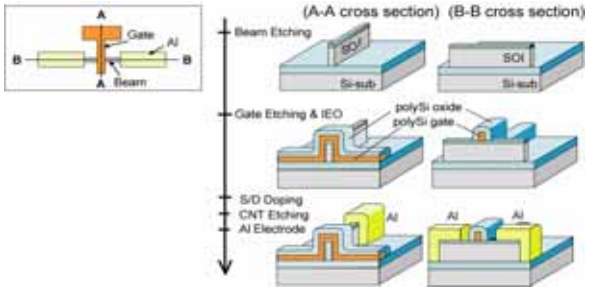
(A-2) Self-aligned oxide coating by impurity-enhanced oxidation.



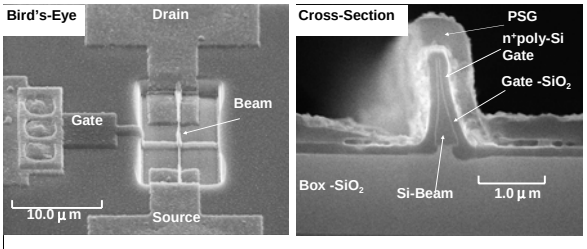
(A-4) Low-resistivity Ni-silicided S/D beam.

Selective oxide coating of silicon gate

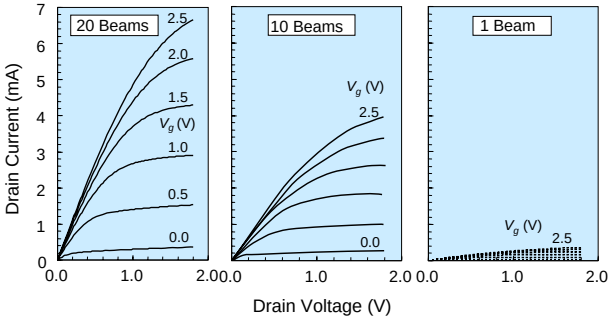
Polysilicon gate is covered with its own oxide utilizing impurity-enhanced wet oxidation at lower than 800°C



Beam-Channel Transistor, BCT



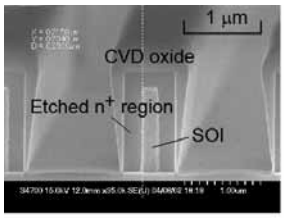
Current drivability of BCT with multi-channels



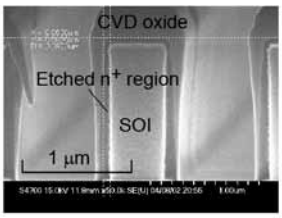
BCT with 10-nm T_{ox}, 0.8-μm L_{eff}, 40-nm W_b, and 1.0-μm H_b.

Conformal n^+ doping with AH_3+Ar plasma

Observed uniformity of doped regions with $POCl_3$-gaseous doping (a) or AH_3+Ar plasma doping (b).



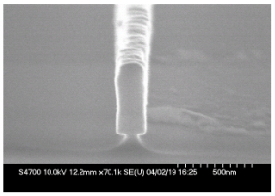
(a) Gaseously doped with $POCl_3$



(b) Plasma doped with AsH_3& Ar

Application of silicided source/drain

Ni-silicide formation on Si beam



Beam height/width＝550 nm/180 nm

Material	Resistivity (Ω-cm)
n^+-Si beam	4.2×10^{-4}
Ni silicided beam	2.5×10^{-5}