Constraint of Source/Drain Formation with Plasma Doping Applied for Beam Channel Transistor on SOI

Kei Kobayashi, Kiyoshi Okuyama, and Hideo Sunami

Research Center for Nanodevices and Systems, Hiroshima University
1-4-2 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8527, JAPAN
Phone: +81-82-424-6265 / Fax: +81-82-424-3499
e-mail: sunami@sxsys.hiroshima-u.ac.jp

1. Introduction

To overcome the short-channel effect, three-dimensional (3-D) transistors, e. g. FINFET[1], have been extensively developed. While, this 3-D structure may facilitate much higher drivability per unit planar area due to its tall vertical channel. According to this feature, two types of beam-channel transistor (BCT) have been successfully developed [2, 3] as shown in Fig. 1. Since the doubled length of silicon beam height is approximately the channel width of MOS transistor, transistor drivability is defined to be propotional to beam height/channel length, H_b/L_{ch}.

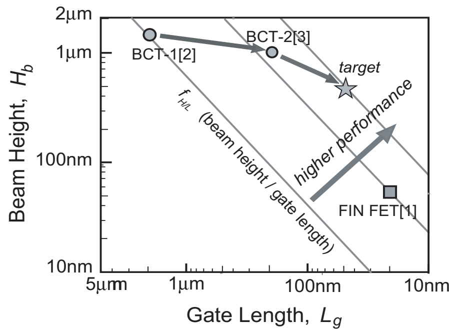

Fig. 1 Strategy for beam-channel transistor (BCT) development with an emphasis on area-conscious application.

To fabricate MOS transistor on tall silicon beam, there exist several issues:(1) high-aspect ratio silicon beam formation, (2) conformal gate formation, (3) uniform source/drain(S/D) formation, and (4) conformal metal contact to S/D. The former two have been intensively studied in our previous works[2-4].

In this presentation, experimental results are shown for an application of plasma doping (PD) to form 1-µm tall and thin S/D. Since oblique implantation is not adequate to obtain uniform doping into deep portion of a narrow silicon trench inbetween ajacent two silicon beams, plasma doping with less directionality may be much more appropriate.

2. Experimental

To form S/D of transistor, deep and heavily doped S/D regions are made at first with $POCl_3$ gaseous doping (GD) at 950ºC. Then, extension regions are formed at r.t by plasma doping (PD) with AsH_3 and Ar gas mixture or the same GD, as shown in Fig. 2. PD is carried out in 2-Pa Ar plasma with a bias of -1000V at 13.56-MHz, 170-W RF power. Then, the substrate is annealed with RTA in nitrogen at 1000ºC for 10 sec. BCT and planar transistor are fabricated on (110)-oriented, 1-µm thick, 50-mm$^{\phi}$ SOI substrate.

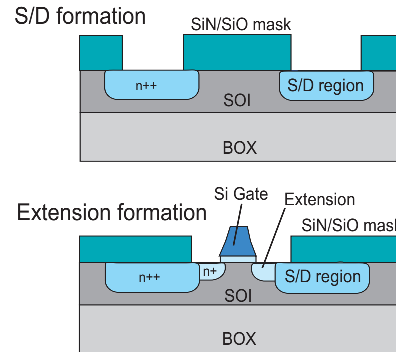

Fig. 2 Process steps for forming n^{++} S/D regions and n^{+} extension regions.

N^+ regions formed with PD or GD are shown in Fig. 3. The doped regions are revealed by preferential etching with a 1:HF+60:HNO_3 mixed solution. Junction depths are approx. 200 nm and 60 nm for GD and PD, respectively. The sheet resistance of the PD region is about 500Ω/❑.

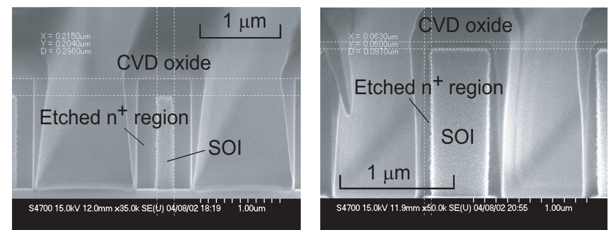

Fig. 3 Observed uniformity of doped regions with $POCl_3$ gaseous doping (a) or AH_3+Ar plasma doping (b).

3. Results and Discussion

A cross section of a typical BCT obtained is shown in Fig. 4. Note that the upper edges of the BCT are strongly rounded. It is speculated in this work that plasma damages which have caused the edge rounding had great influences on device failures described hereafter.

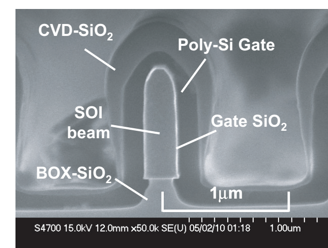

Fig. 4 Obtained beam-channel transistor with plasma doping.

A crude classification of device failures is summarized in Fig. 5. It is characterized that the gate leakage only ocurred in BCT however, open contacts of aluminum metallization happened for both BCT and planar. This is because aluminum electrondes climb over 1-μm tall SOI step and become unconnected at the bottom edge of SOI for both BCT and planar transistor even with substrate heating at 400ºC expecting conformal covering of aluminum film. Since SOI beam is etched with tetra methyl ammonium hydroxide, vertical surface is atomically flat (111) surface. Furthermore, hazardous undercut occurred below SOI beam.

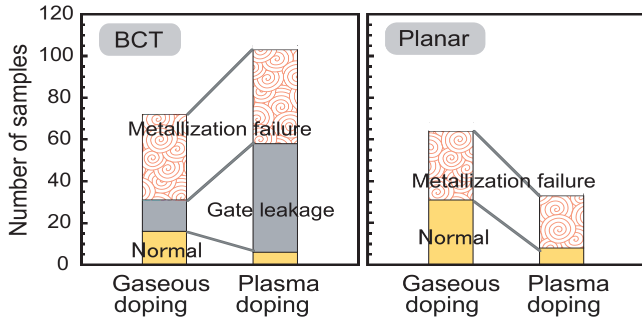

Fig. 5 A crude classification of device failures.

Thicknesses of BCT and planar gate oxides simultaneously formed are 9 nm and 13 nm, respectively, because the BCT gate oxide is formed on (111) face and that of planar, (110).

Detailed distributions are shown in Fig. 6. Major reason why transconductance of BCT with GD widely varies is that gate oxide was anomalously thickened due to narrow process window associated with the BCT formation process.

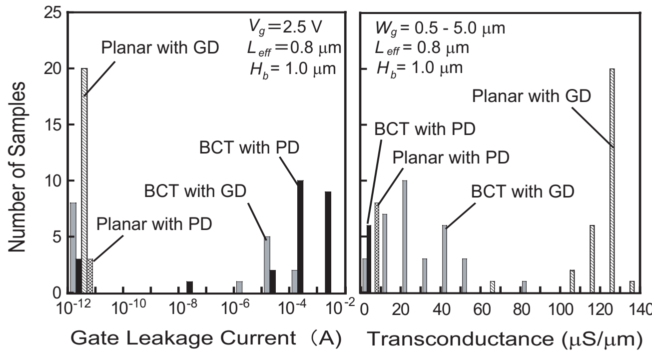

Fig. 6 Failure and performance distributions for BCT

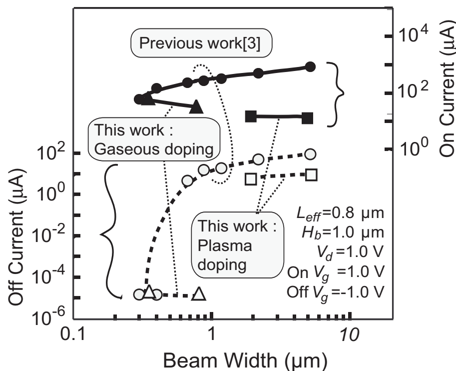

Fig. 7 Device performance comparison in terms of on- and off-drain currents.

Summarized device performance is shown in Fig. 7 focusing on on- and off-drain currents of BCT and planar transistor. In addition, typical I_d-V_g characteristics are shown in Fig. 8. In gaseous doping case, normal performance is obtained however, plasma doping gives birth to anomalouslly low performance.

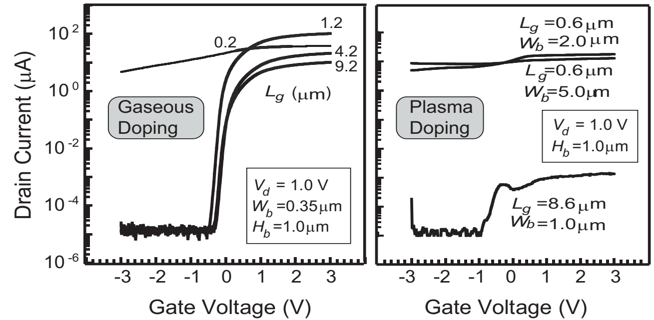

Fig. 8 Typical I_d-V_g characteristics of BCT with gaseous or plasma dopings.

As previously discussed, it was already recognized that the Ar plasma doping used in this study caused silicon sputtering resulting in rounded top edges of SOI beam[5]. The influence of the sputtering energy is also recognized on device performance in terms of gate leakage and transconductance degradation.

4. Conclusion

Plasma doping is first applied to the fabrication of beam-channel transistor (BCT) on 1-μm thick (110) SOI substrate. Almost desirable performance is obtained for BCT with $POCl_3$ gaseously doped extension region however, that with plasma doped extension is anomalouslly degraded. It is estimated that plasma damages cause degradation of the device performance, gate leakage and transconductance lowering in particular.

Further investigation should be carried out to quantitatively analyze these damages and to solve these issues utilizing damage-free doping technique. Also much more conformal contact metallization, such as CVD conductive material, should be applied in order to achieve reliable tall 3-D transistors.

Acknowledgements

This work was partly supported by Grant-in-Aids for Scientific Research (B#12555102, A(2)#13025232) from the Ministry of Education, Science, Sports, and Culture, Japanese Government.

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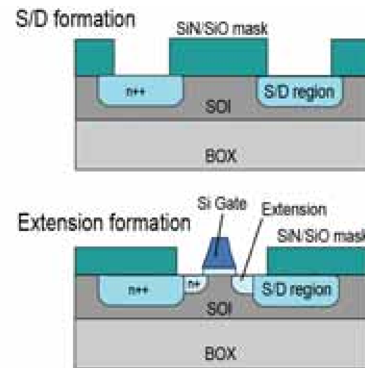
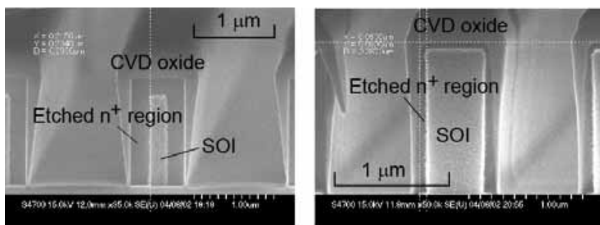
Process steps for forming S/D

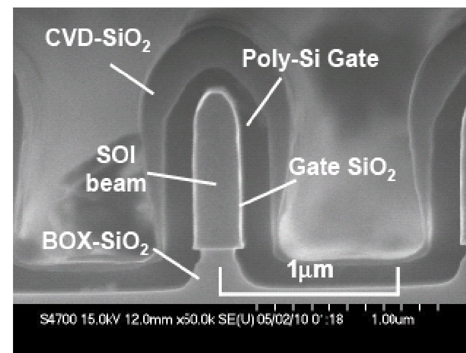


Uniformity of doped region on a Si beam

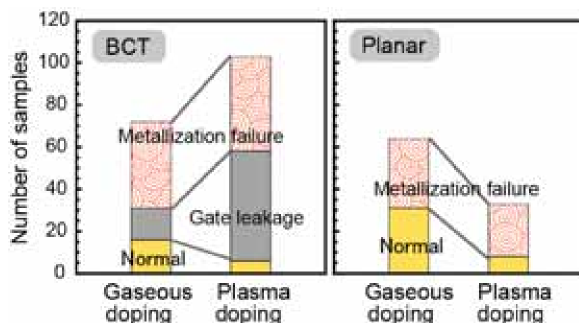


(a) Gaseously doped with $POCl_3$ (b) Plasma doped with AsH_3 & Ar

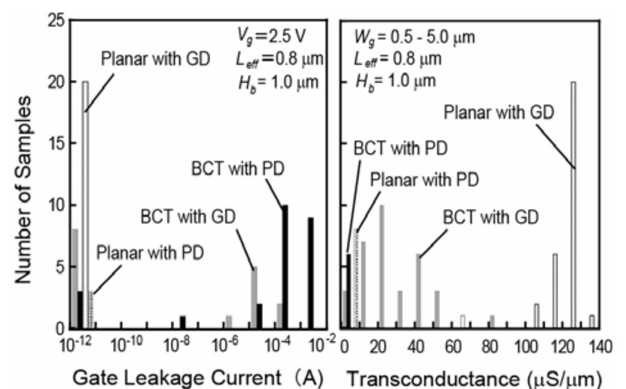
Obtained Beam Channel Transistor



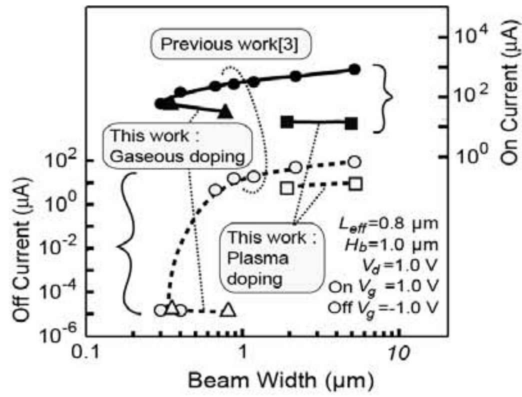
Crude classification of device failures



Failure and performance distributions



On- and off-currents distributions



Typical I_d – V_g characteristics