Characterization of Newly Developed 3-D Parallel-Triple Gate MOS Transistor

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1. Introduction

It is known that double gate structure has advantage to control the short channel effect as compared with conventional bulk devices. Three-dimensional (3-D) device structure such as FinFET that realize double gate structure vertically have been developed [1]. On the other hand, for 3-D devices with vertical channel, drive current per unit planer area can be increased with the increase in the beam height. In this viewpoint, 3-D transistor with higher aspect ratio such as beam channel transistor (BCT) [2] and corrugated channel transistor (CCT) [3] have been proposed and successfully fabricated. Thus, there are some possibilities to utilize advantage of 3-D structure. Then, the progress of new structure and/or new operation is important. In this report, a new vertical structure transistor is proposed.

The structure of proposed device is shown in Fig. 1. In this structure, three transistors that are formed on a SOI beam can operate independently. This can apply to parallel part of a logic circuit, for example a part of NAND gate. Since transistors are integrated vertically, this structure has an advantage from the viewpoint of area efficiency.

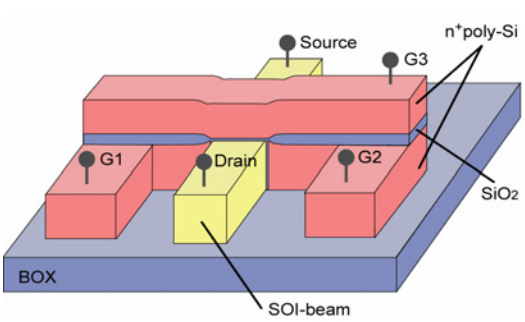

Fig. 1 A proposed device that has three independent gate electrodes.

In the fabrication of this device, it is important to form three gate electrodes using self-aligned process to realize tight compaction. The fabrication process is devised in consideration of this point. The process sequence is shown in Fig. 2. Formation of isolation layer for gate electrodes, and leveling of poly-Si are key techniques to realize the proposed device.

2. Device fabrication

Boron-doped SOI wafers of 10 Ω-cm in resistivity are used as starting material. After formation of SOI beams with 250 nm in height by reactive ion etching (RIE) and gate oxide film on the sidewall by thermal oxidation, poly-Si is deposited by thermal chemical vapor deposition and doped with phosphorous by $POCl_3$ gasses. The resistivity of the n^+poly-Si film is almost $5x10^{-4}$ Ω-cm. Subsequent leveling of n^+poly-Si is achieved by chemical mechanical polishing (CMP). Multi-layer films consist of thermal oxide, n^+poly-Si, and Si_3N_4 are deposited on the planarized surface for the top gate electrode formation. After patterning of gate electrodes and etching processes, formation of isolation layer that separates poly-Si wirings is needed. Since gate oxide film of the top gate and the isolation layer of gate electrodes are formed simultaneously, it is important to enlarge the ratio of oxide thickness of Si substrate and poly-Si. From this reason, the impurity enhanced oxidation (IEO[4]) is introduced. Oxide thicknesses of phosphorous doped n^+poly-Si and boron doped Si are shown in Fig. 3. The ratio of oxide thickness exceeds almost 4.4 times at 850 °C while it is about 2.7 times at 1000 °C. The former condition is adopted in this fabrication process. After the IEO, n^+poly-Si deposition, and its leveling by CMP etch-back, top gate electrodes are covered with its own oxide by thermal oxidation. Side-gate electrodes are formed by RIE utilized the top gate as an etching mask.

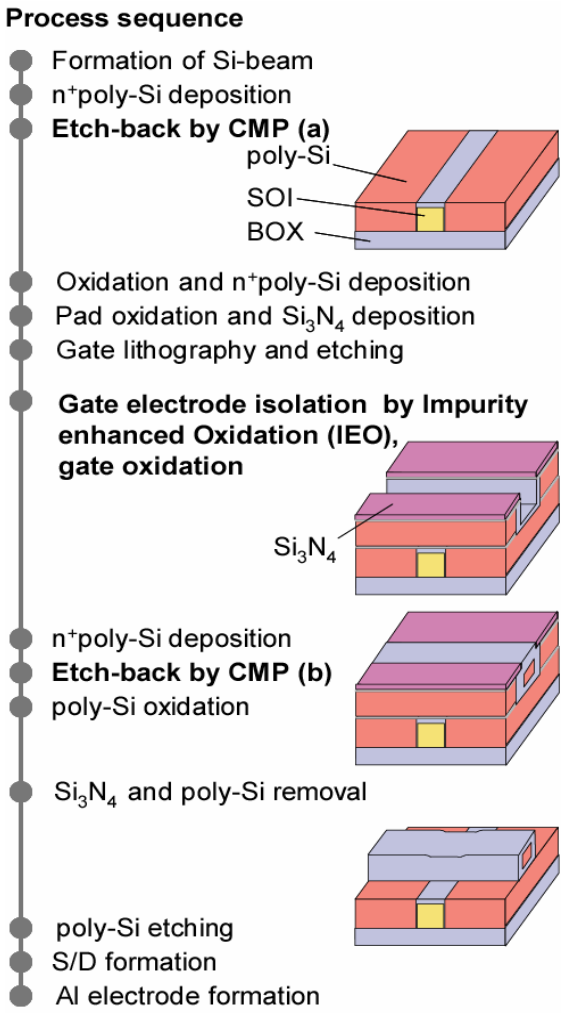

Fig. 2 The process sequence of the proposed device.

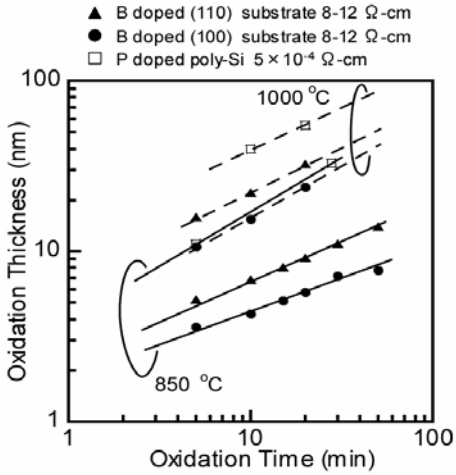

Fig. 3 Impurity enhanced oxidation at 850 °C and 1000 °C (O_2 = 2 slm).

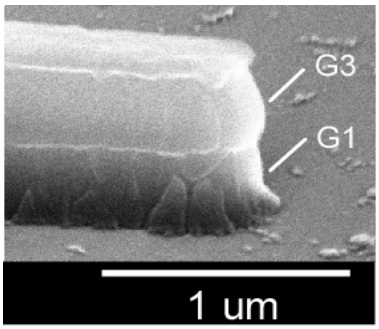

Fig. 4 An SEM image of two layer n^+poly-Si wiring with 300-nm width.

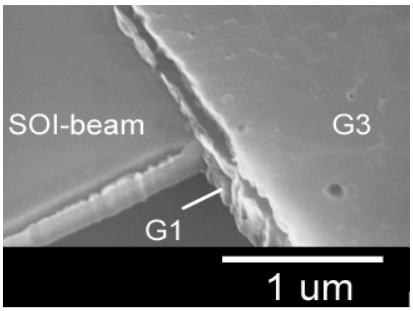

Fig. 5 A bird's eye view of the fabricated device. Side-gate electrode (G1) and top one (G3) are formed successfully on an SOI beam.

The proposed triple gate structure was successfully fabricated as shown in Figs. 4 and 5. Subsequent source and drain formation is achieved by arsenic ion implantation and rapid thermal annealing.

3. Characterization and Discussion

I_d-V_g characteristics of fabricated 3-D parallel-triple gate transistor are shown in Fig. 6. While no channel implantation causes weak cut-off, gate voltage of other gates are fixed -1.0 V in the measurement. Thus, normal operation of each transistor is confirmed. The drain current of top gate (G3) is 2.8 times at V_d = 1.0 V than that of side gate (G1 and G2) since the aspect ratio of devise is about 0.5. Measurements on various beam width are in progress.

4. Summary

A novel 3-D Transistor structure is proposed and successfully fabricated utilizing the IEO and CMP etch-back. Normal operation of each transistor is confirmed. Characterization on several conditions is in progress.

5. References

[1] Y-K. Cho, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Andersen, T-J. King, J. Bokor, and C. Hu, IEDM Tech. Dig., pp. 421-424, 2001.

[2] A. Katakami, K. Kobayashi, and H. Sunami, Jpn. J. Appl. Phys., Vol. 43, No. 4B, pp. 2145-2150, 2004.

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[4] H. Sunami, J. Electrochem. Soc., **125,** pp. 892-897, 1978.

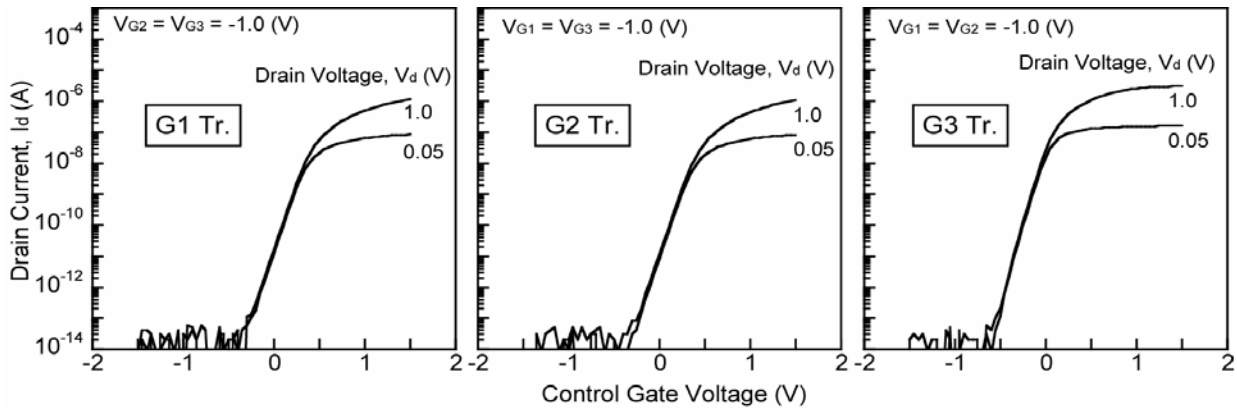

Fig. 6 I_d-V_g characteristics for parallel-triple gate transistor with 250 nm in height and 540 nm in width SOI beam and 4-um gate length.

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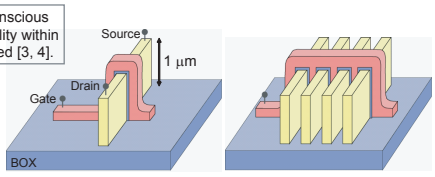
Hiroshima University

Introduction

It is known that double gate structure has an advantage to control the short channel effect as compared with conventional bulk devices. 3-D devices such as FinFET [1] and tri-gate transistor [2] with multi-gate structure have been proposed and developed as candidates for further scaled MOS devices in future.

Besides the scaling, some area-conscious applications resulting in large drivability within small planer area have been proposed [3, 4].



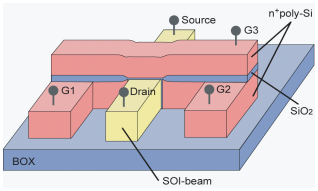
Beam channel transistor [3] Corrugate channel transistor [4]

Objectives : Development of transistor structure and its formation process for appropriate application of 3-D transistor

In this report, a new 3-D MOSFET with novel fabrication process is proposed

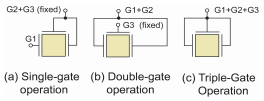
Proposed device

Parallel-Triple Gate MOS Transistor



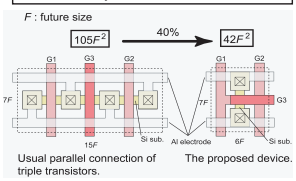
Three gate electrodes formed on an SOI beam Independently

Operation Modes



(a) Single-gate operation (b) Double-gate operation (c) Triple-Gate Operation

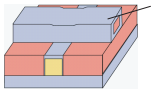
For parallel-connected three transistor operation, This device has an advantage from the viewpoint of area efficiency.



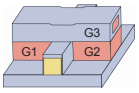
Usual parallel connection of triple transistors. The proposed device.

Fabrication process

Formation of G1 and G2 using a G3 pattern

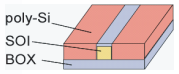


Anisotropic dry etching

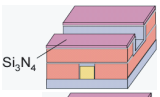


Process sequence

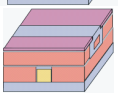
- Formation of Si-beam by RIE
- n+poly-Si deposition
- Etch-back by CMP (a)



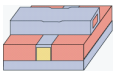
- Oxidation and n+poly-Si deposition
- Pad oxidation and Si3N4 deposition
- Gate lithography and etching by RIE
- Formation of isolation layer by Impurity enhanced oxidation (IEO [5])



- Gate oxidation
- n+poly-Si deposition
- Etch-back by CMP (b)
- Poly-Si oxidation

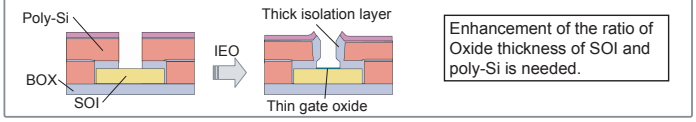


- Si3N4 and poly-Si removal
- Side-gate formation by RIE
- S/D formation by ion implantation
- Al electrode formation

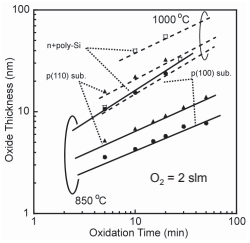


Experimental

Gate electrode isolation by the impurity enhanced oxidation [5]



Enhancement of the ratio of Oxide thickness of SOI and poly-Si is needed.



Ratio of oxide thickness

p(100) substrate : P doped poly-Si

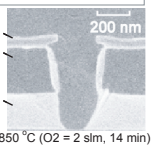
850 °C	1 : 4.4
1000 °C	1 : 2.7

The ratio exceeds almost 4.4 at 850 °C

Resisitivity

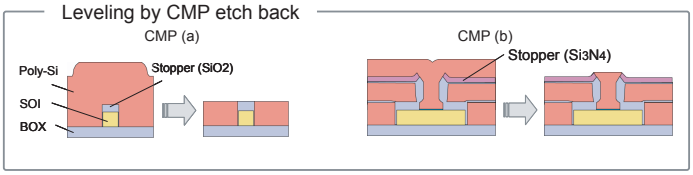
P doped n+poly-Si : 5x10-4 (Ω-cm)

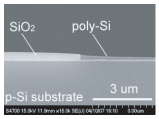
B doped p(100) and p(100) sub. : 8-12 (Ω-cm)



IEO at 850 °C (O2 = 2 slm, 14 min)

Leveling by CMP etch back

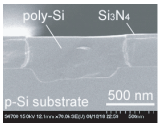




Areas of SOI-beams are narrow in this process.

Dummy patterns are introduced to prevent dishing and erosion.

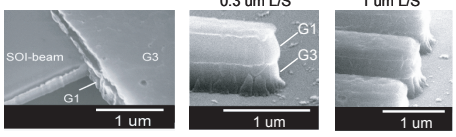
A layout patterns with dummy



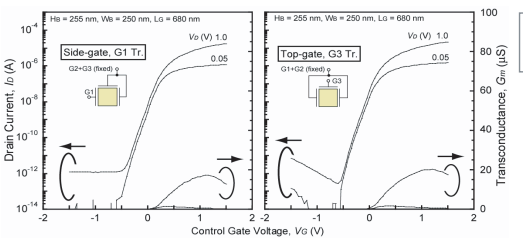
A good configuration is obtained.

Result

Obtained gate structures



I_D-V_D characteristics



Normal operations on single-gate mode for each gate are confirmed.

The gate voltage of other two gates is fixed at -1.0 V.

Gate oxide thicknesses
G1 and G2 : 4.8 nm
G3 : 4.7nm
(No channel implantation)

Summary

A novel 3-D transistor structure and its fabrication process are proposed. In this process, G1 and G2 are delineated using a G3 pattern as an etching mask.

The impurity enhanced oxidation and CMP etch back are introduced in this fabrication.

- **The impurity enhanced oxidation : The oxide thickness ratio exceeds almost 4.4 at 850 °C**
- **CMP etch back : Dummy patterns are introduced to prevent dishing and erosion.**

The proposed device is successfully fabricated on novel self-aligning techniques using these processes and normal operations on single-gate mode for each gate are confirmed.

References

[1] Y-K. Cho, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Andersen,T-J. King, J. Bokor, and C. Hu, IEDM Tech. Dig., pp. 421-424, 2001.
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