Characterization of Charge Trapping and Dielectric Breakdown of HfAlOx/SiON Dielectric Gate Stack

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1 Introduction

Hf-based silicates and aluminates showing good thermal stability [1] and favorable energy-band alignment [2] have been intensively studied as most promising alternative gate dielectrics. Despite a number of efforts to improve the dielectric properties of such high-k thin films, reliability issues such as charge trapping and dielectric wear-out are still matters of research [3, 4], especially for metal-gate/high-k dielectric gate stack.

In this work, we have focused on a $HfAlO_x$ (Hf/(Hf+Al)=~0.3)/SiON stack structure and studied its temperature dependence of leakage current from Al-gate, charge trapping properties and time-dependent dielectric breakdown (TDDB).

2 Experimental

After standard wet-cleaning of 300mm p-type Si(100) wafers, a 1.2nm-thick oxynitride interfacial layer (IL) was formed by a process sequence of NH_3 anneal at 700°C and subsequent oxidation at 850°C in NO ambience. $HfAlO_x$ (Hf/(Hf+Al)=~0.3) films in the thickness range of 3-7nm were deposited on IL by an atomic layer CVD (ALCVD) method, in which trimethy-aluminum, tetrakis ethyl- methylamino hafnium and water were used as precursors and NH_3-plasma treatment was performed at each cycle of ALCVD. The post-deposition anneal was performed at 1000°C for 1sec in 0.2% O_2 diluted by N_2. Finally, Al gates with a diameter of 0.5mm were formed on top by evaporation.

3 Results and Discussion

3.1 Current Conduction Mechanism

The leakage current through 3nm-thick $HfAlO_x$/SiON at negative gate voltages beyond –1.5V agrees well with direct tunneling (DT) current simulated in an energy band alignment determined by XPS measurements [5] (Fig. 1). For the cases with 5nm-thick and 7nm-thick $HfAlO_x$, Frenkel-Poole (FP) emission of trapped electrons dominates the current leakage at voltages beyond –2.0V, and the dielectric constant (~$10\varepsilon_0$) evaluated from the slop of the FP plot on the leakage current is slightly smaller than the value (~$12\varepsilon_0$) determined from the accumulation capacitances. The observed I-V hysteresis and anomalous leakage current in the gate voltage region below -1.0V for each case are interpreted in terms of electron trapping and de-trapping at defect states in the dielectric stacks. The strong temperature dependence of leakage currents as shown in Fig. 2 is attributed to an FP emission process from traps localized at 0.7-0.8eV from the conduction band (Fig. 3). Notice that the anomalous leakage current at lower voltages is eliminated when temperatures rises to ~100°C presumably by thermal re-emission of trapped electrons. The fairly weak temperature dependence of the leakage for the 3nm-thick $HfAlO_x$ case is also attributed to the transport due to DT.

3.2 Charge Trapping Characteristics

A decrease in the leakage current during constant voltage stress (CVS) is observable for each case until soft breakdown (SBD) occurs (Fig. 4). The result is attributable to the defect generation and electron trapping at generated defects. [6]. The net positive charges during CVS are differently changed in different $HfAlO_x$ thicknesses (Fig. 5), which can be interpreted by a model as schematically illustrated in Fig. 6. In the model, the defect generation during CVS results electron trapping in $HfAlO_x$ near the gate side and hole trapping near $HfAlO_x$/SiON interface and/or in the SiON interfacial layer. The negative flat-band voltage shift caused by hole trapping at sites far from the gate is more efficient than the positive flat-band voltage shift by electron trapping near the gate. With decreasing the dielectric thickness, namely, the distance between the trapped electrons and holes, the net sheet charge in the dielectric stack is reduced in this model. For HfAlOx as thin as 3nm (Fig.6(a)), the neutralization of trapped holes with injected electrons and hole detrapping may happen. The enhanced electric field near the HfAlOx/SiON interface by charge trapping and resultant recombination electron and hole near the interface during CVS appears to trigger soft breakdown.

3.3 TDDB Characteristics

The TDDB characteristics for the first current jump (soft breakdown) during CVS as seen in Fig. 4 were measured at different stress voltages and temperatures, and characterized by Weibull distribution. With decreasing the $HfAlO_x$ thickness, the Weibull slop is markedly decreased (Fig. 7), being similar to the case of SiO_2. Although the time-to-SBD (t_{SBD}) is shorten with increasing stress voltage and temperature irrespective of conduction mechanism being dominated by DT or FP emission, the Weibull slope remains unchanged with stress voltage and temperature. We derived the field acceleration factor from the slop of natural logarithmic t_{SBD} at 63% failures vs electric field in $HfAlO_x$ and plotted as a function of temperature (Fig. 8.) For the case with 3nm-thick $HfAlO_x$, the field acceleration factor shows no clear temperature dependence, while for a thicker $HfAlO_x$ case the acceleration factor is remarkably decreased with increasing temperature higher than ~60°C. Obviously, the field acceleration factor reflects the temperature dependence of electron transport through the

dielectric stack. For the FP case, increased current flow with temperature is major cause of SBD and the field assistance for emission of trapped carriers at higher temperatures becomes less important. In contrast, for the DT case, increased charge trapping and/or defect generation rate with thermal vibration is responsible for shortened t_{SBD}.

4 Summary

For Al/HfAlOx/SiON/Si(100) stack structures, the leakage current at high negative gate voltages is dominated by direct tunneling for the case with 3nm-thick $HfAlO_x$ and by the Poole-Frenkel emission for the cases with thicker $HfAlO_x$. During CVS for the gate injection, electron and hole trapping in the dielectric stack proceeds near the Al gate and Si(100), respectively. For the direct tunneling case, the field acceleration factor of TDDB shows no significant temperature dependence, but for the FP emission cases it decreases at temperatures above ~60 °C. The charge trapping in the dielectric stack is a major factor to characterize the dielectric breakdown.

Acknowledgement

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References

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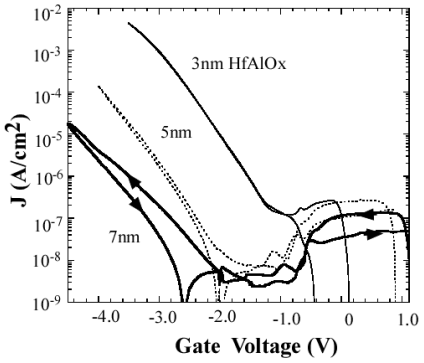

Fig.1 Current-voltage (I-V) characteristics for the capacitors with different $HfAlO_x$ thicknesses. The simulated I-V curves are also shown as references.

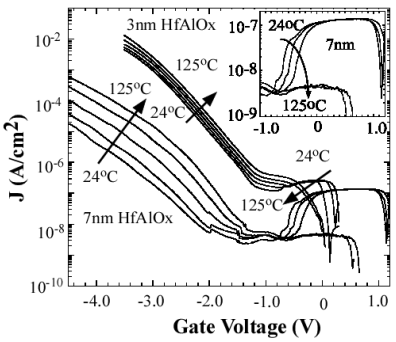

Fig. 2 I-V characteristics measured at different temperatures.

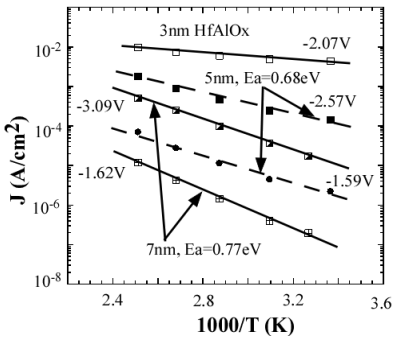

Fig. 3 Arrhenius plots of leakage currents at different gate voltages.

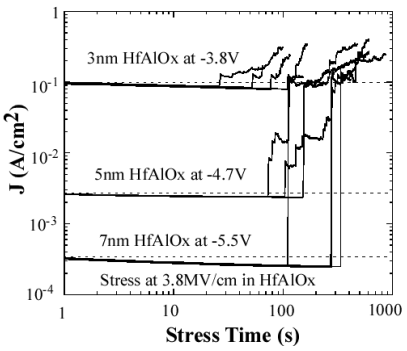

Fig. 4 Temporal changes in current density during constant-voltage stress. The electric field was fixed at 3.8MV/cm in $HfAlO_x$

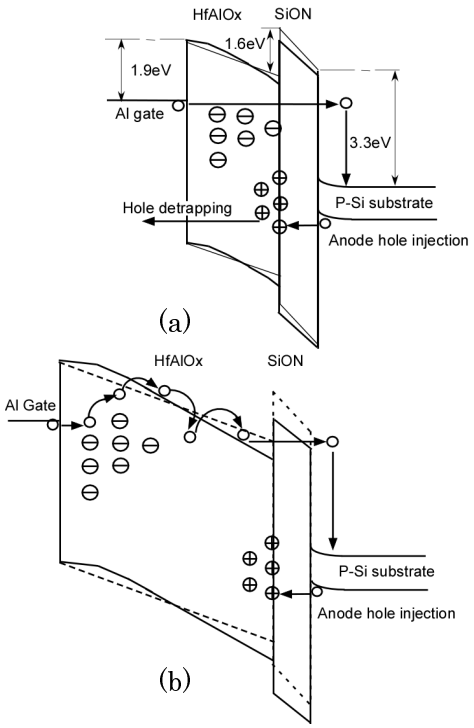

Fig .6 Energy band diagram with charge trapping during CVS to the capacitors (a) with 3nm-thick $HfAlO_x$ (b) 7nm-thick $HfAlO_x$.

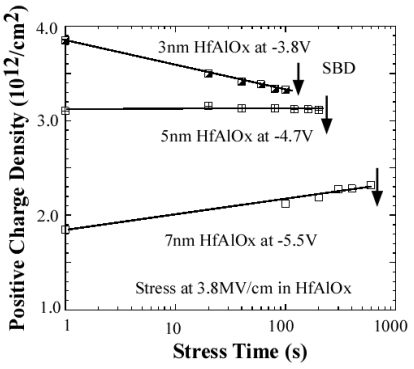

Fig. 5 Changes in net positive charges density as a function of stress time under 3.8MV/cm in $HfAlO_x$.

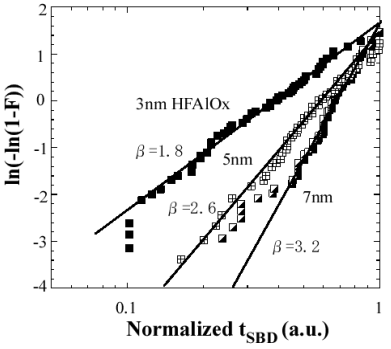

Fig. 7 Weibull plots of time to SBD. The time to SBD was normalized by its maximum.

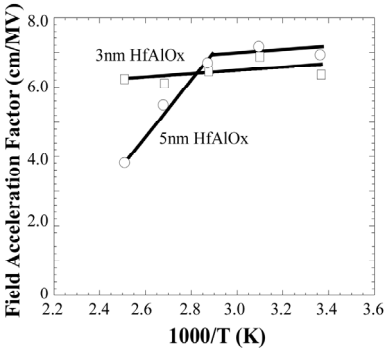

Fig .8 Field acceleration factor as a function of temperature.

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OUTLINE

Back Ground

- Hf-based aluminates
  - Favorable energy-band alignment
  - $E_{g(HfAlOx)}$=6.5eV, ΔE_c=1.78eV
  - Excellent thermal stability
  - Against crystallization>900 °C

⇨ Promising alternative gate dielectrics

- Eliminate poly-Si gate depletion
- Release the Fermi-level pinning

⇨ Application of metal gate on MOSFETs with High-K

Major concern : Reliability

Poly-Si gate ⇨ Breakdown mechanism, Reliability

K. Torii: IEDM (2004), VLSI(2004)
W. Mizubayashi: APL(2004)

This work

Metal (Al, Ni and Au)/HfAlOx/SiON/p-Si(100) MOS Capacitor

Charge Trapping, TDDB

Fabrication of MOS Capacitors

300mm p-Si(100) ~10 Ω·cm

- Wet-Cleaning
- Nitridation 700°C, NH_3
- Oxidation NO

1.2nmSiON / P-Si(100)

- ALCVD : $HfAlO_x$ [Hf/(Al+Hf)=0.3] (3~7nm)

Precursors: $Hf[N(C_2H_5)CH_3]_4$, $Al(CH_3)_3$, H_2O,

$HfAlO_x$ / 1.2nmSiON / P-Si(100)

With NH3-plasma treatment at each cycle of ALCVD

- PDA : 0.2% O_2 in N_2 1000°C:1sec
- Metal Gate (Al, Au and Ni) Φ 0.5mm

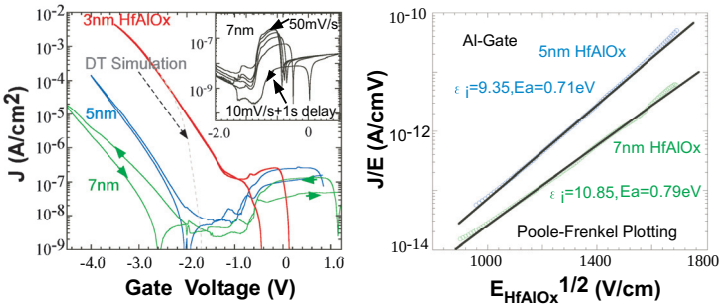
Metal Gate (Φ 0.5mm) / $HfAlO_x$ / 1.2nmSiON / p-Si(100)

MEASUREMENTS

- Current-Voltage (I-V)
  Capacitance-Conductance-Voltage (C-G-V)
  Constant Voltage Stress (CVS)

Leakage Current Characteristics
Charge Trapping Characteristics
TDDB Characteristics

I-V Characteristics of Al/HfAlOx/SiON Capacitors

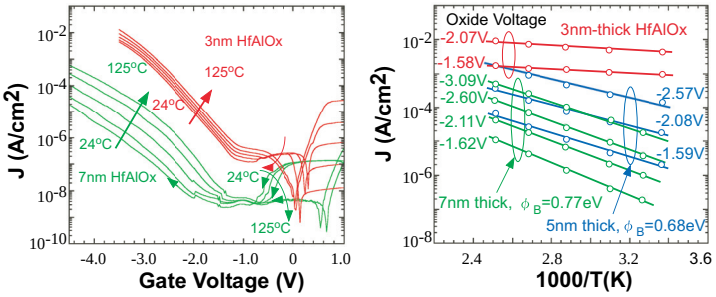


Capacitors with 3nm-thick HfAlOx: DT tunneling current

Capacitors with 5 or 7nm-thick HfAlOx: Poole-Frenkel conductive mechanism

Anomalous leakage current at lower voltages: Electron charge trapping and detrapping

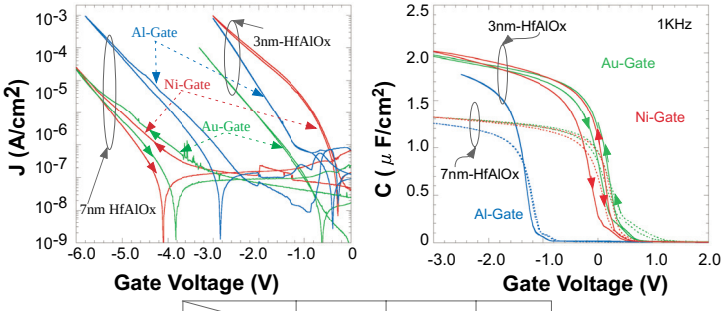
I-V Temperature Characteristics of Al/HfAlOx/SiON Capacitors



Energy Level of Charge Trapping:

7nm-thick HfAlOx: 0.77eV 5nm-thick HfAlOx: 0.68eV

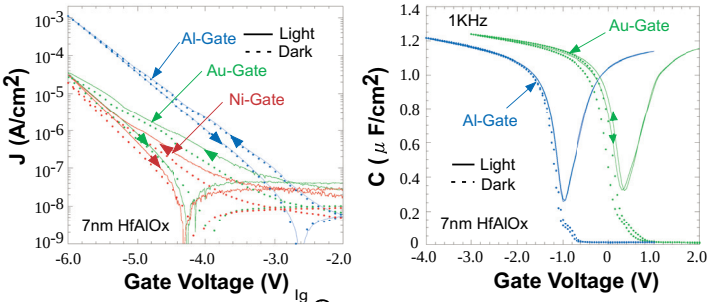
C-V and I-V Characteristics of Metal/HfAlOx/SiON Capacitors

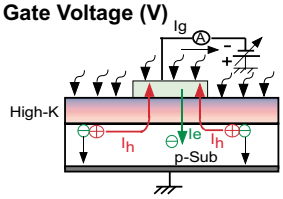


	Al	Ni	Au
ΔV_{FB} (3nm)(V)	-0.35	0.30	0.32
ΔV_{FB} (7nm)(V)	-0.30	0.32	0.34

Positive Fixed Charge Negative Fixed Charge

I-V and C-V Characteristics Under Cold Light and In Dark

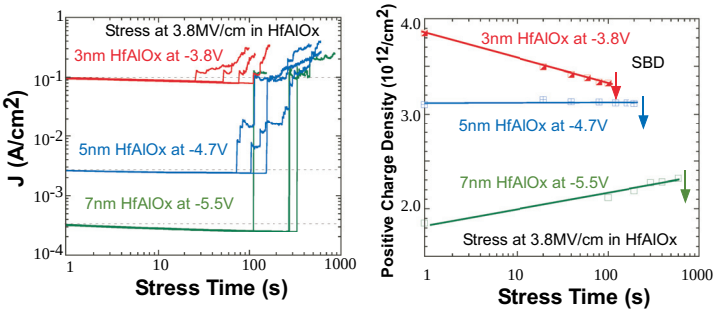




Al electrode: Electron current

Au and Ni electrode: Hole current

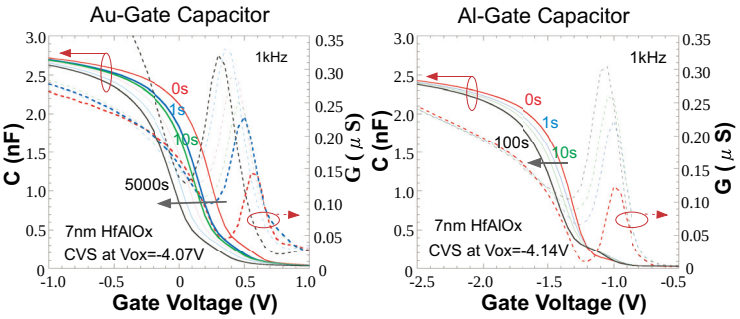
Thickness Dependence of Charge Trapping Characteristics for Al-Gate Capacitors



Decreasing of leakage current as stress time indicates the electron trapping near gate.

The change of net positive charge density is dependent on HfAlOx thickness.

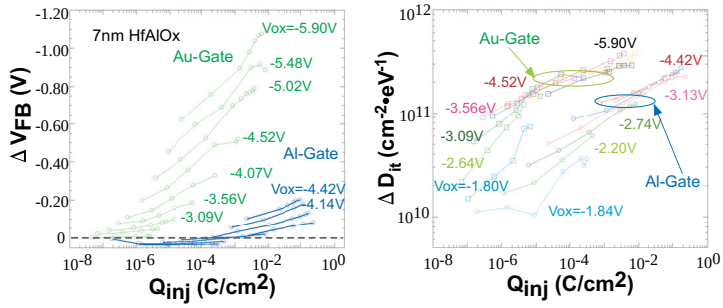
Flat Band Shift and Conductance Change under CVS for Al and Au Gate Capacitors



The negative flat band shift and conductance change with stress time of CVS were observed.

For Au gate capacitors, the negative flat band shift is more significant than Al gate capacitors.

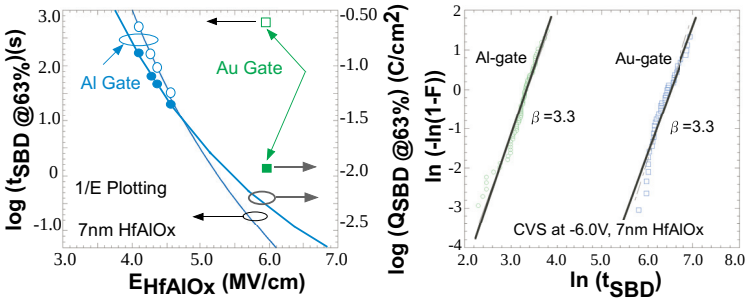
Change of Flat Band Shift and Interface State Density with Injected Charges



Au-Gate capacitors: The flat band shift is larger than Al-Gate case by several folds.

A stress field dependence of ΔD_{it} becomes weak with increasing of Q_{inj}, and tend to be saturated.

t_{SBD} and Q_{SBD} Characteristics

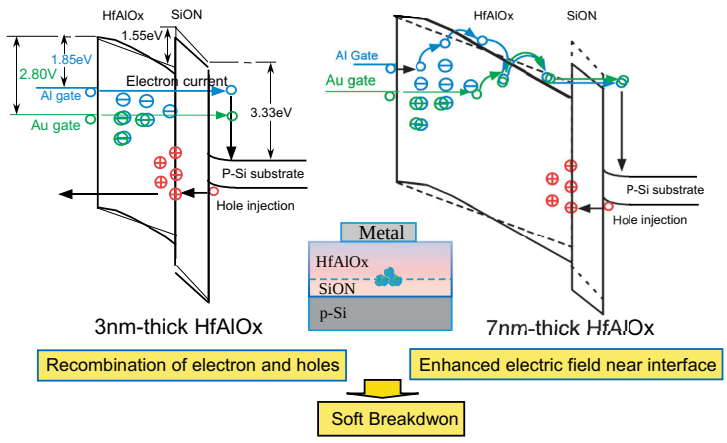


The soft breakdown (SBD) was attributed to the charge trapping generated in the stack film.

Au-gate Capacitors: Both of t_{SBD} and Q_{SBD} are increased, indicating a lower defect generation rate.

The same Weibull slope (β ~3.3) indicates the same breakdown mechanism.

Energy Band Diagram with and without Charge Trapping

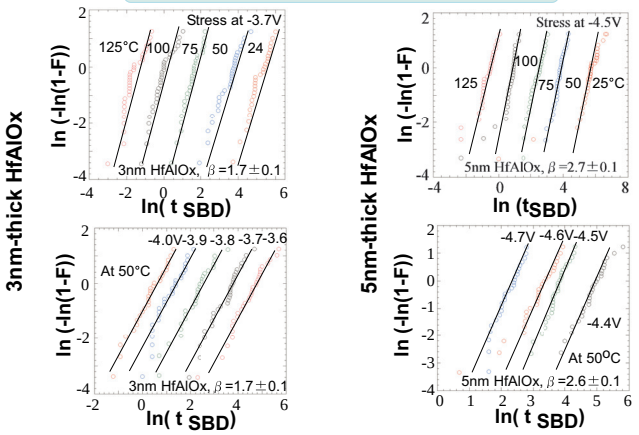


Recombination of electron and holes

Enhanced electric field near interface

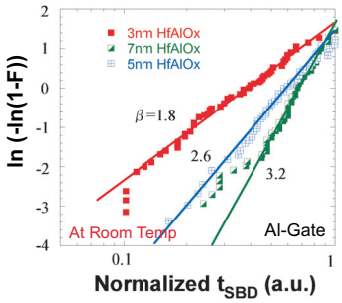
Soft Breakdwon

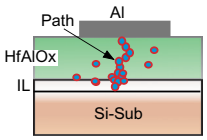
Weibull Plots of SBD for Al-Gate Capacitors



The Weibull slope is independent on the temperatures and stress voltages.

Thickness Dependence of Weibull Plots

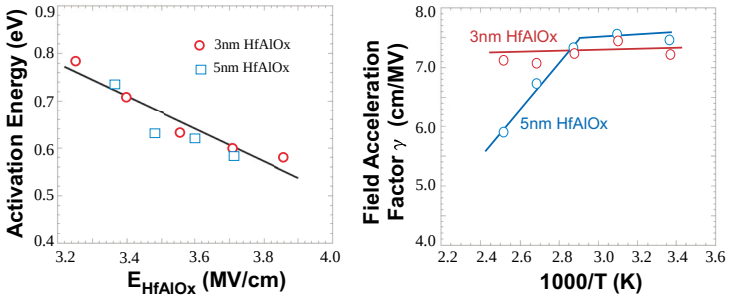




Percolation Model for SBD

The Weibull slope is increased as increase of HfAlOx thickness.

Thermal Activation Energy and Field Acceleration Factor for SBD of Al-Gate Capacitors



Ea --- 5.8~7.8eV (3.2~3.9MV/cm)

Ea= ΔH_0-C E (ΔH0*=1.85eV, C=0.34)*

Breaking Bond:

Hf-O (~801.7kJ/mol) and Si-O (~800kJ/mol)

$$t_{BD} \propto \frac{Qcrit}{J(T, Eox)\,\alpha\,(T, Eox)}$$

$$\gamma = \frac{\partial \ln t_{BD}}{\partial Eox} = \frac{\partial \frac{1}{J(T, Eox)\,\alpha\,(T, Eox)}}{\partial Eox}$$

Summary

- Leakage Current Characteristics:
  - Al-Gate Capacitor : Electron Current is dominate
  - Au-Gate Capacitor : Hole current contributes to the leakage current

  DT (3nm-thick HfAlOx)
  PF (5 or 7nm-thick HfAlOx)
- Charge Trapping Characteristics:
  - The electron trapping and hole trapping are generated near metal gate and interface of HfAlOx/SiON by electron and hole current respectively.
  - Energy band distortion and release energy due to charge chapping and recombination may play a role on the soft breakdown.
- Soft Breakdown:
  - TDDB Weibull slope which independent on the field and temperature of stress is increased with increasing the thickness of HfAlOx.
  - The temperature dependence of TDDB is associated with major contribution of pre-existing traps, especially at the interface between the HfAlOx and SiON layers, to the breakdown path formation.

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