Characterization of MultiStep Electron Charging to Silicon-Quantum-Dot Floating Gate by Applying Pulsed Gate Biases

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1. Introduction

The implementation of silicon-quantum-dots (Si-QDs) as a floating gate in metal-oxide-semiconductor field-effect-transistors (MOSFETs) has been attracting much attention because of its feasibility for multivalued memory operations at room temperature [1-4]. So far, we have fabricated nMOSFETs with a Si-QDs floating gate and confirmed multistep threshold voltage shift due to Coulomb blockade effect at Si-QDs at room temperature [1, 4]. We have also demonstrated that electron charging of the Si-QDs floating gate at constant gate voltages proceeds stepwise through metastable charged states associated with the redistribution of injected electrons [4]. From the activation energy of injection time and metastable state, we have suggested that electron transfer between different energy states of neighboring Si-QDs plays an important role on multistep charging characteristics. Such unique multistep charging has yet to be studied in details to control precisely discrete charged states in the Si-QDs.

In this work, to gain a better understanding of the mechanism of multistep electron charging in the Si-QDs floating gate, we have studied the transient characteristics of the drain current after charging of Si-QDs floating gate at different pulsed gate biases.

2. Experimental

n-MOSFETs with a floating gate of doubly-stacked Si-QDs were fabricated by the following process steps. Hemispherical and single-crystalline Si-QDs were self-assembled on a 3.3-nm-thick SiO_2 layer thermally grown on p-Si(100) by controlling the early stages of LPCVD of pure SiH_4 at 575°C. After that a 1-nm-thick thermal oxide layer was grown at 850°C, and the second Si-QDs layer was deposited under the same conditions. The average dot height and the dot density evaluated by AFM were 6nm and $6\times10^{11}cm^{-2}$, respectively. Subsequently, a 3.3-nm-thick amorphous Si layer was uniformly grown on the dot layer by LPCVD of 10% Si_2H_6 diluted with He at 440°C and fully oxidized in dry 2% O_2 to form a 7.5-nm-thick control oxide. Finally, n^+poly-Si gate and source/drain junction were fabricated. The gate length and width were 0.5 and 10μm, respectively.

3. Results and Discussion

Figure 1 shows temporal changes in the drain current measured after application of single-pulsed gate biases at a base gate voltage of 0V. The drain current drops to the minimum value immediately after the application of pulsed gate bias. The minimum drain current corresponds to the amount of electrons injected by the pulse gate bias. As shown in Fig. 2, the minimum drain current decreases stepwise with increasing pulse height at different base gates voltages and correspondingly the threshold voltage shifts increase in a staircase pattern, which indicate the multistep charging in Si-QDs floating gate due to the Coulomb blockade effect. Note that the threshold-voltage shift at each of the charging steps decrease with progressive electron charging. This implies that the Coulomb

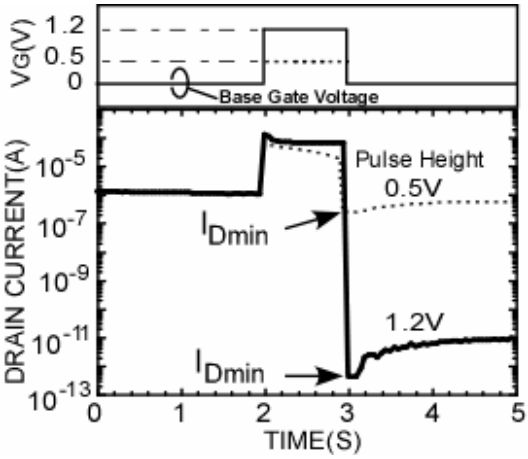

Fig. 1. The temporal changes in the drain current for writing operations by applying a single-pulsed gate biases of 0.5 or 1.2V.

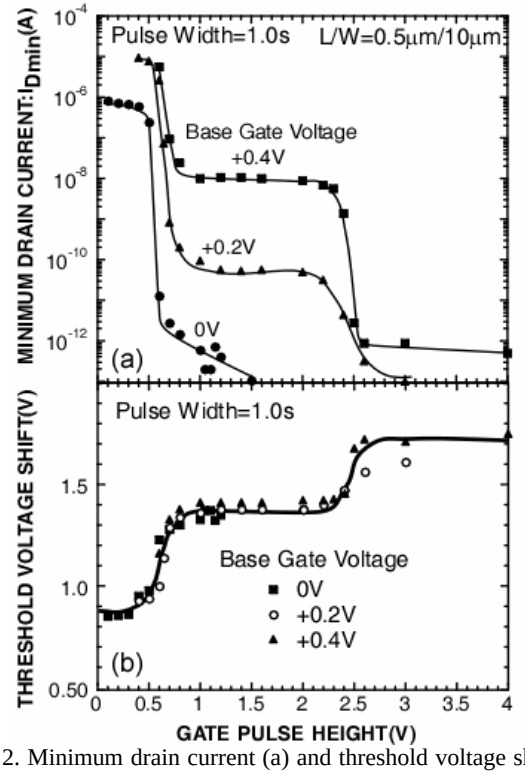

Fig. 2. Minimum drain current (a) and threshold voltage shift (b) as a function of gate pulse height at base gate voltages of 0, 0.2 and 0.4V. The pulse width was constant at 1.0s.

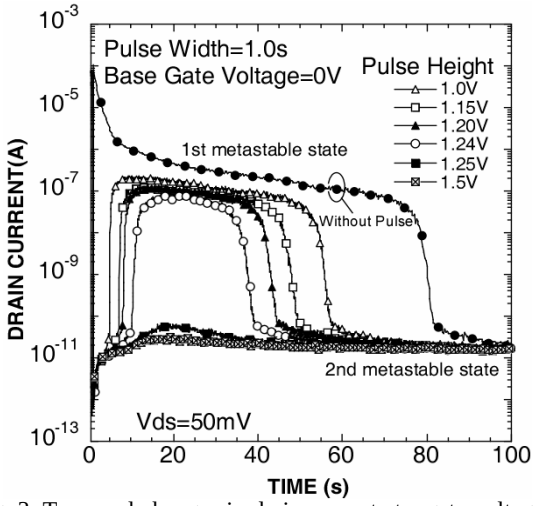

Fig. 3. Temporal changes in drain current at a gate voltage of 0V and a drain voltage of 50mV after applying different pulse gate biases. The pulse height was varied in the range of 1.0-1.5V at a pulse width of 1s.

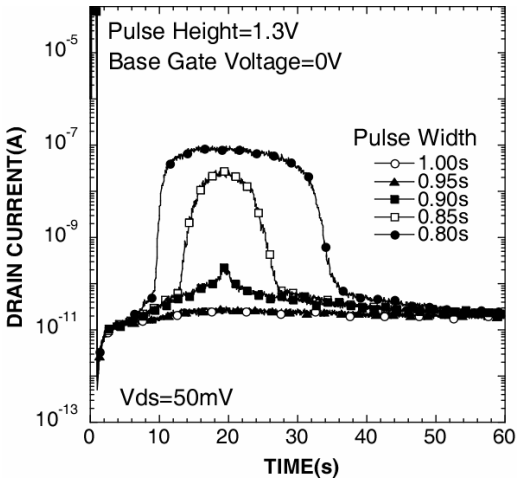

Fig. 4. Temporal changes in drain current at a gate voltage of 0V and a drain voltage of 50mV after applying different pulse gate biases. The pulse width was varied in the range of 0.8-1.0s at a pulse height of 1.3V.

interaction among the neighboring charged Si-QDs contributes to an increase in the charging energy of the QDs.

To get a clear insight into the charged states, the temporal change in the drain current were measured at a constant gate voltage of 0V after electron injection to the 2nd (metastable) state by applying the gate pulse bias as shown in Fig. 3. In the cases with a pulse height of 1.24V and below, the drain current rapidly increases to some current level and then decreases as seen in the electron injection without pulse except shorten time to the 2nd injected state. The increase in drain current means the emission of electrons stored in unstable charged state of Si-QDs floating gate. The metastable state in which the drain current slightly decrease with time is attributed to the redistribution of injected electrons in the Si-QDs floating gate [4]. The period of the metastable state decreases with the pulse height. When the pulse height is increased only by 10mV from 1.24V to 1.25V, an increase in the drain

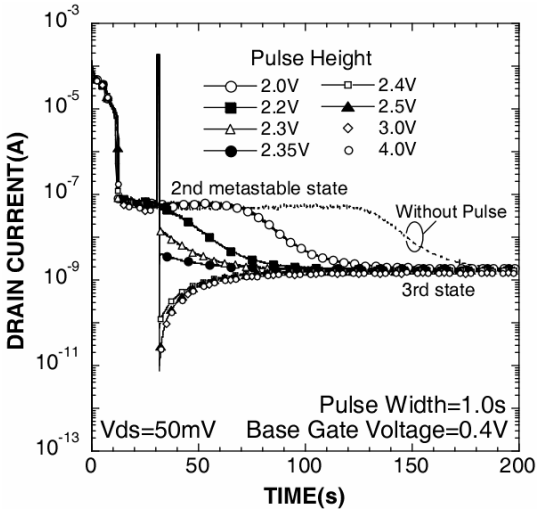

Fig. 5. Temporal changes in drain current at a voltage of 0.4V and a drain voltage of 50mV. Pulse gate biases with various heights at a constant width (1s) were applied in the 2nd metastable state.

current due to the electron emission with time becomes hardly observable, which indicates that injected electrons settle at a stable condition at V_G=0V. A similar result was obtained in the I_D-t characteristics after applying pulsed gate bias at different pulse widths at constant pulse height as shown in Fig. 4, where the electron emission after injection at a pulse height of 1.3V is observable within 0.90s in pulse width. The results of Fig. 3 and 4 indicate that pulse height and width are crucial factors for the charge distribution in the metastable state even though the amount of injected charge is the same at each pulse height.

Figure 5 shows the temporal change in the drain current at V_G=0.4V, where pulse biases with different heights were applied to the gate in the 2nd metastable state. The period of the 2nd metastable state is markedly shorten with pulse height. When the pulsed bias exceeds 2.2V, the electron injection to the final state proceeds without any metastable state. In addition, when the pulse height is increased from 2.35V to 2.4V, an over-charged state is realized as seen in the electron emission after the application of pulsed bias, which indicates the Coulomb blockade to the final state becomes insignificant at conditions over a critical bias.

Summary

The temporal change in the drain current after applying pulsed gate biases confirms the redistribution of electrons in the Si-QDs floating gate during the metastable state which involves a reduce in the effective charging energy and a release of Coulomb brocade.

Acknowledgement

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Outline

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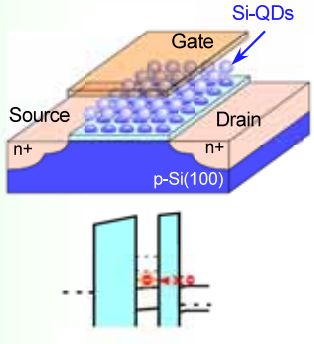
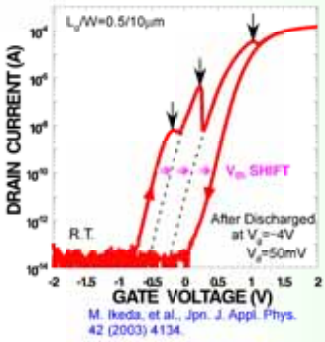
Background



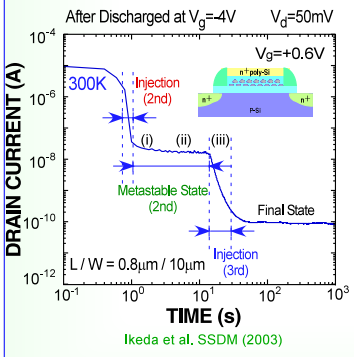


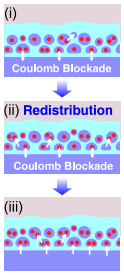
- Coulomb Blockade
- Quantum Confinement

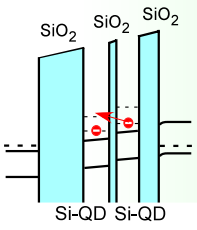
Multivalued Memory Operation at Room Temperature

S. Tiwari, et al., Appl. Phys. Lett. 68 (1996) 1379.

Our Previous Work

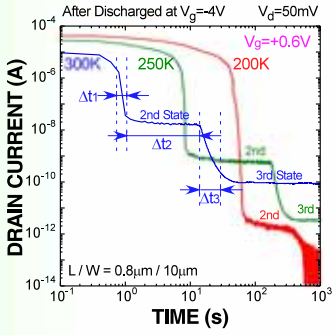


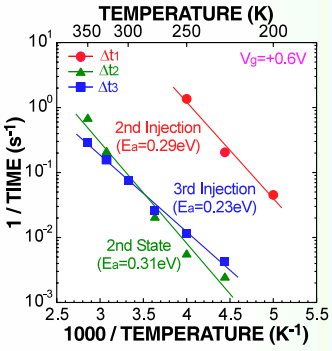




Ikeda et al. SSDM (2003)

Temperature dependence of the I_d-t Characteristics



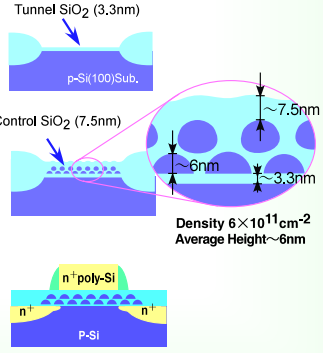


This Work

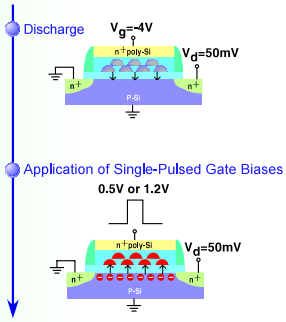
We have studied the charging and discharging characteristics of the Si-QDs floating gate by applying various pulsed gate biases.

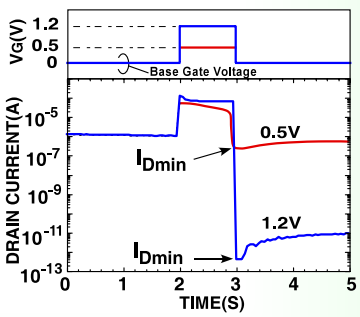
Fabrication of Si-QDs Floating Gate n-MOSFETs

- p-well & LOCOS
  $N_A = 1.5 \times 10^{17} cm^{-3}$
- Oxidation (Tunnel SiO_2)
  2%Dry O_2, 1000℃
- 0.1%HF Treatment
- Si-QDs Formation by LPCVD
  SiH_4 (100%) : 575℃, 0.2Torr, 60sec
- Oxidation of Si-QDs Surface
  2%Dry O_2, 850℃
- a-Si Deposition & Oxidation (Control SiO_2)
  a-Si Deposition (3.3nm)
  Si_2H_6 (10% in He) : 440℃, 0.2Torr
  a-Si Oxidation
  2%Dry O_2, 1000℃
- Gate Fabrication
  n^+poly-Si Thickness = 200nm
  L / W = 0.5μm / 10μm
- Source/Drain Implantation



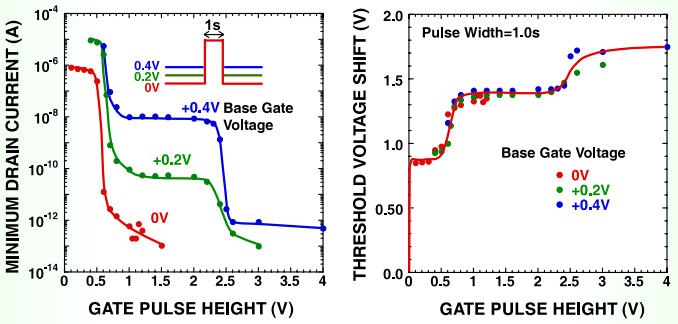
I_d-t Characteristics by Applying Single-Pulsed Gate Biases





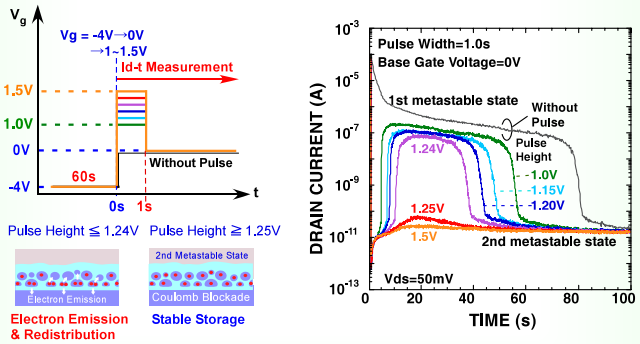
- Electron injection in the Si-QDs floating gate by pulsed gate biases results in the minimum drain current.

Minimum Drain Current and Threshold Voltage Shift as a Function of Gate Pulse Height



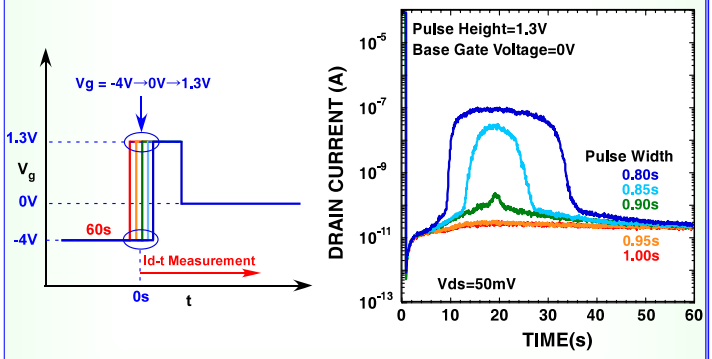
- The minimum drain current decreases stepwise with increasing pulse height at different base gates voltages. About the threshold voltage shift, we see that it increases in a staircase pattern independent of the base gate voltage.

I_d-t Characteristics after Applying Pulsed Gate Biases at Different Pulse Heights



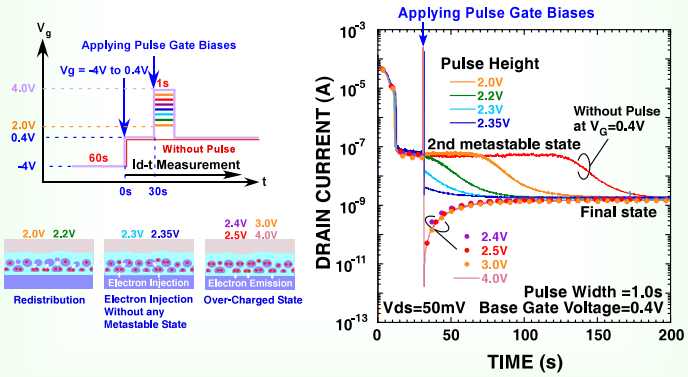
- When the pulse height is increased only by 10mV from 1.24V to 1.25V, an increase in the drain current due to electron emission with time becomes hardly observable.

I_d-t Characteristics after Applying Pulsed Gate Biases at Different Pulse Widths



- When the pulse width is increased only by 50ms from 0.90s to 0.95s, the electron emission with time becomes hardly observable.

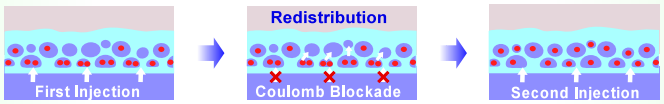
I_d-t Characteristics after Applying Pulsed Gate Biases at Different Pulse Heights in the 2nd Metastable State



SUMMARY

- **The temporal change in the drain current after applying pulsed gate biases confirms the redistribution of electrons in the Si-QDs floating gate during the metastable state.**

The redistribution of electrons in the Si-QDs floating gate during the metastable state involves a reduce in the effective charging energy and a release of Coulomb brockade.



Acknowledgements

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