Characterization and application of SiON gate dielectrics

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1. Introduction

In this COE project, the subject of our group is research and development of future reliable gate dielectrics. The subject includes atomic-layer-deposition (ALD) of silicon nitride, ALD high–*k* gate dielectrics, and plasma nitrided SiON gate nitride, etc. This time, we present the results of SiON gate dielectrics. Namely, the application of ALD Si nitride/SiO_2 gate dilectrics to future scaled DRAM and bias temperature instability (BTI) characteristics of a MOSFET with plasma nitrided SiON gate dielectric under high-frequency bipolar gate bias.

2. Application of ALD Si niutride/SiO_2 gate dielectrics to future DRAMs

ALD of Si nitride is one of the key technologies for the next generation gate dielectrics [1,2]. ALD Si-nitride/SiO_2 stack gate dielectrics were applied to high-performance transistors for future scaled DRAMs [3]. The stack gate dielectrics of the peripheral PMOS transistors excellently suppress boron penetration. ALD stack gate dielectrics exhibit only slightly worse negative-bias temperature instability (NBTI) characteristics than pure gate oxide (Fig. 1). Enhanced reliability in NBTI was achieved compared with that of plasma-nitrided gate SiO_2 (Fig.1). Memory-cell (MC) NMOS transistors with ALD stack gate dielectrics show slightly smaller junction leakage than those with plasma-nitrided gate SiO_2 in a high-drain-voltage region, and have identical junction leakage characteristics to transistors with pure gate oxide [3]. MCs having transistors with ALD stack gate dielectrics and those with pure gate oxide have the identical retention-time distribution [3]. Taking the identical hole mobility for the transistors with ALD stack gate dielectrics to that for the transistors with pure gate oxide both before and after hot carrier injection [2] into account, the ALD stack dielectrics are a promising candidate for the gate dielectrics of future high-speed, reliable DRAMs.

3. BTI characteristics under high-frequency bipolar gate bias

NBTI of p-MOSFETs with ultrathin SiON gate dielectric has been investigated under various gate bias configurations [4-6]. The NBT-induced interface trap density (ΔN_{it}) under unipolar bias is essentially lower than that under static bias, and is almost independent of the stress frequency up to 10 MHz (Fig.2). On the contrary, ΔN_{it} under bipolar pulsed bias of frequency larger than about 10 kHz is significantly enhanced and exhibits a strong frequency dependence (Fig.3), which has faster generation rate (Fig.4) and smaller activation energy as compared to other stress configurations. The enhancement was found to be mainly governed by the fall time (t_F) of the pulse waveform (Fig. 5), namely, the transition time of the silicon surface potential from strong accumulation to strong inversion, rather than the pulse rise time (t_R) and the pulse duty factor (D). The enhancement decreases significantly with t_F increasing, and is almost eliminated when t_F is larger than ~ 60 ns. The degradation enhancement is attributed to the recombination of free holes and trapped electrons at the SiO_2/Si interface and/or near interface states upon the quick shift of the silicon surface potential reversal from accumulation to inversion.

4. Conclusion

ALD stack dielectrics are a promising candidate for the gate dielectrics of future high-speed, reliable DRAMs. New findings of enhancement of BTI degradation are presented in MOSFET with plasma nitrided SiO_2 gate dielectrics under high –frequency bipolar gate bias,

References

[1] Anri Nakajima, Hiroyuki Ishii, and Shin Yokoyama, "Carrier Mobility in Metal-Oxide-Semiconductor Field Effect Transistor with Atomic-Layer-Deposited Si-Nitride Gate Dielectrics," Jpn. J. Appl. Phys. Vol. 44, No. 28 pp. L903–L905, July (2005).

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[3] Anri Nakajima, Takuo Ohashi, Shiyang Zhu, Shigeyuki Yokoyama, Shigetomi Michimata, and Hideharu Miyake, "Atomic-Layer-Deposited Si-Nitride/SiO_2 Stack Gate Dielectrics for Future High-Speed DRAM with Enhanced Reliability," IEEE Electron Device. Lett. Vol. 26, No. 8, pp. 538-540, August (2005).
[4] Shiyang Zhu, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake, "Interface Trap Generation Induced by Charge Pumping Current under Dynamic Oxide Field Stresses, " IEEE Electron Device. Lett. Vol. 26, No.3, pp. 216-218, March (2005).
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[6] Shiyang Zhu, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake, "Pulse Waveform Dependence on Ac Bias Temperature Instability in pMOSFETs," IEEE Electron Device. Lett. Vol. 26, No. 9, pp. 658-660, Sept. (2005).

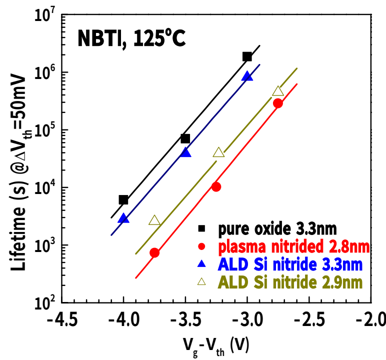

FIG.1 Device lifetime as a function of stress field at 150 °C for peripheral PMOS transistors with L/W=1μm/10μm.

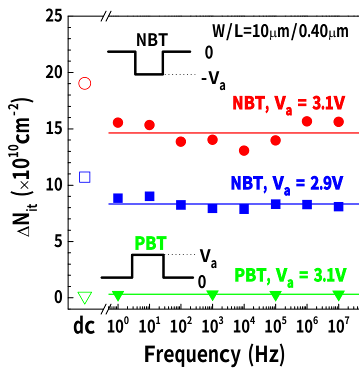

FIG.2 Interface trap generation ΔN_{it} as a function of stress frequency at different stress voltage V_{stress}, under unipolar pulsed stress (L=0.40μm) for a pMOSFET with plasma-nitrided SiO_2 gate dielectrics. Stressed at 125°C for 10^3s. The data of dc stresses are also shown for comparison, whose nominal stress time is 500s. Inset is a schematic waveform applied on the gate.

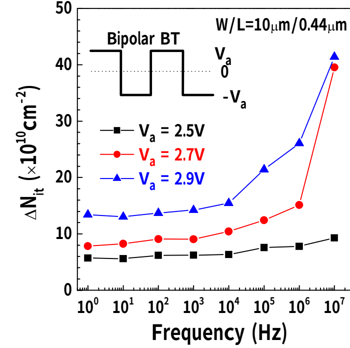

Fig.3 Interface trap generation ΔN_{it} as a function of stress frequency at different stress voltage V_{stress}, under bipolar pulsed stress (L=0.44μm) for a pMOSFET with plasma-nitrided SiO_2 gate dielectrics. Stressed at 125°C for 10^3s.

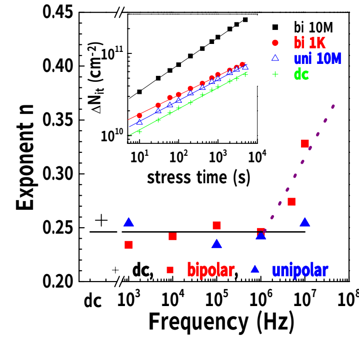

FIG.4 The exponent n of the ΔN_{it} time power function as a function of stress frequency at unipolar and bipolar pulsed stresses. The data of dc stress is also given for comparison. Inset is the time evolution of ΔN_{it} for four typical stresses. The exponent n was extracted from the linear fitting of these plots.

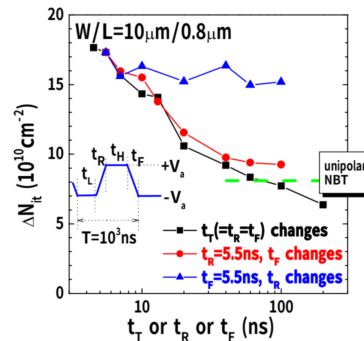

FIG.5 Interface trap generation ΔN_{it} as a function of t_R (or t_F) under bipolar stresses at 10^6 Hz with a trapezoidal waveform. Inset shows a schematic waveform to define t_L, t_R, t_H and t_F for a pMOSFET with plasma-nitrided SiO_2. Devices have size of W/L= 10μm/0.8μm and are stressed at 125°C for 10^3s. For comparison, ΔN_{it} under unipolar stress with a square waveform ($t_T = t_R = t_F = 4.5$ ns) is also shown.

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1. Introduction

- In this COE project, the subject of our group is research and development of future reliable gate dielectrics:
  - SiON gate nitride including atomic-layer-deposition (ALD) of silicon nitride.
  - ALD high–*k* gate dielectrics.
- This time, we present the results of SiON gate dielectrics:
  1. Application of ALD Si nitride/SiO_2 gate dielectrics to future scaled DRAM
  2. Bias temperature instability (BTI) characteristics of a MOSFET with plasma nitrided SiON gate dielectric under high-frequency bipolar gate bias.

2. Application of ALD Si niutride/SiO_2 gate dielectrics to future DRAMs

This work has been published in
IEEE Electron Device. Lett. Vol. 26, No. 8, pp. 538-540 (2005).

background

- ALD Si-nitride/SiO_2 stack gate dielectrics shows excellent suppression of boron penetration.
- ALD Si-nitride/SiO_2 stack gate dielectrics shows excellent dielectric breakdown characteristics.
- Heavy thermal budget is necessary to DRAM fabrication process.

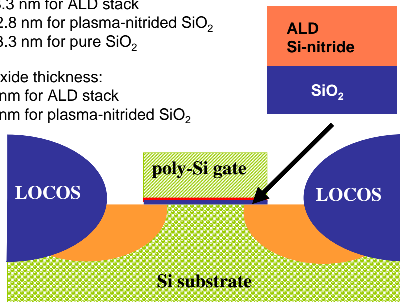
purpose

- To evaluate applicability of ALD stack gate dielectrics to DRAM, device characteristics are systematically investigated.

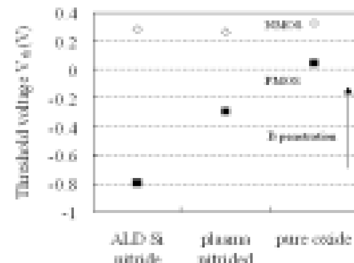
• *Experimental*

EOT : 3.3 nm for ALD stack
2.8 nm for plasma-nitrided SiO_2
3.3 nm for pure SiO_2

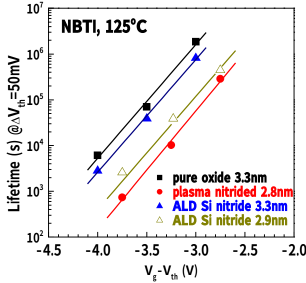
Base oxide thickness:
2.0 nm for ALD stack
3.5 nm for plasma-nitrided SiO_2



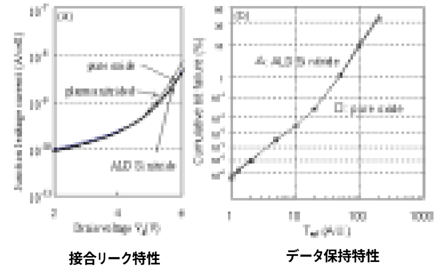
V_{th} of peripheral NMOSFETs and PMOSFETs



Device lifetime as a function of V_g-V_{th}



Memory cell characteristics



Summary:

- ALD stack gate dielectrics have a special advantage of suppression of boron penetration over plasma-nitrided gate SiO_2 and pure gate oxide.
- ALD stack exhibit enhanced reliability in NBTI compared with plasma-nitrided gate SiO_2.
- ALD stack shows identical junction leakage current and better characteristics than plasma-nitrided gate SiO_2.
- ALD stack shows identical retention characteristics to pure gate oxide.
- ALD stack is a promising candidate for gate dielectrics of future high-speed and high-reliability DRAMs.

3. BTI characteristics under high-frequency bipolar gate bias

This work has been published in

IEEE Electron Device. Lett. Vol. 26, No.3, pp. 216-218 (2005).

IEEE Electron Device Letters, Vol. 26, No.6, pp.387-389 (2005).

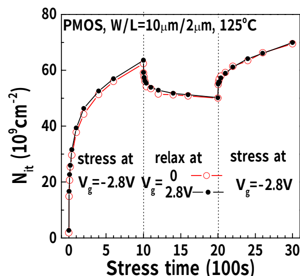
IEEE Electron Device. Lett. Vol. 26, No. 9, pp. 658-660 (2005).

Background:

- NBTI of pMOSFETs is a critical reliability issue for modern CMOS devices.

  dynamic NBT stress is smaller than that under *static* NBT stress due to the partial recovery during the "off" state.

- However, we found the frequency-dependent ***degradation enhancement under bipolar BT stress.***

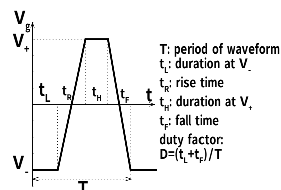


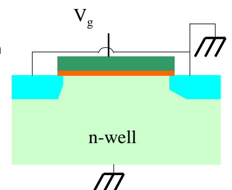
Experimental details:

Devices: pMOSFETs with p+ poly-Si gate, plasma-nitrided SiON gate.

T_{ox}=2.0nm, N%=12%, W=10μm, L=0.28 ~ 0.44μm.

Stress:



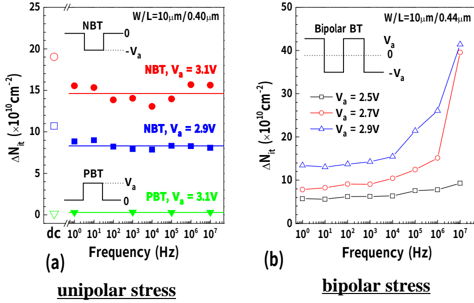


Measurement: A modified **DCIV** method for N_{it}, I_d-V_g for V_{th}.

Results and discussion:

Behaviors of degradation under bipolar BT stress – 1:

unipolar & bipolar

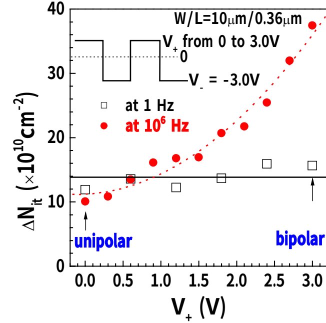


unipolar stress

bipolar stress

Behaviors of degradation under bipolar BT stress – 2:

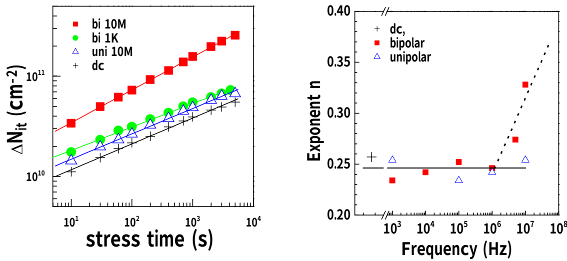
V_+ effect: V_+ from 0 (unipolar stress) to $-V_a$ (bipolar stress), V_- is fixed at –3.0V



Behaviors of degradation under bipolar BT stress – 3:

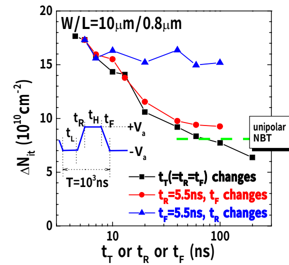
Time evolution of ΔN_{it} under various stress configurations

$$\Delta N_{it} = C \cdot t^n$$



Behaviors of degradation under bipolar BT stress – 5:

ΔN_{it} as a function of t_R (or t_F) under bipolar stresses at 10^6 Hz



summary:

- The device degradation under high-frequency bipolar BT stress is significantly enhanced.
- ΔN_{it} under high-frequency bipolar BT stress has a faster generation rate and smaller activation energy than that under other stress configurations.
- ΔN_{it} increases with decreasing pulse fall time.
- The enhancement is originated from the quick reversal from $+V_a$ to $-V_a$, namely, from accumulation to inversion.

4. Conclusion

- ALD stack dielectrics are a promising candidate for the gate dielectrics of future high-speed, reliable DRAMs.
- New findings of enhancement of BTI degradation are presented in MOSFET with plasma nitrided SiO_2 gate dielectrics under high –frequency bipolar gate bias.