Technology Challenges for Future CMOS

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Escalating needs for information processing and communication in the ubiquitous network society have driven continued progress in LSI technologies. The MOSFET scaling principle [1] has long been powerful for extending the transistor performance in terms of the speed and density. This is because the device electrical parameter tolerance has so far been in the range of maintaining the scaling scenario. As a consequence the transistor architecture and the base materials have remained almost unchanged over the past three decades.

In the recent technology nodes, however, the subthreshold leakage current and exponential gate tunneling current have become real roadblocks which limit continued CMOS scaling , because of increasing standby power dissipation. Thus, extensive R&D efforts are being made to accelerate the device technology shift to implementing new materials and novel structures into integrated devices (Fig.1).

In order to enhance the carrier transport properties in CMOS on the basis of sub-band structure engineering including strain effects, the channel must be designed by optimal combination of crystal surface orientations, channel directions, strain configurations and channel materials such as Si, SiGe and Ge, in addition to multi-gate structures which improve the electrostatics of the devices [2]. Also, metal/high-k gate stack engineering focusing on the threshold voltage adjustment or the effective workfunction control is one of key issues in CMOS technology. The Fermi level pinning (FLP) associated with high-k dielectrics [3] could be relaxed by reducing the number of dipoles induced at the metal silicide /high-k interfaces [4,5] or by modulating the charge neutrality level through the compositional changes of high-k layer [6].

A new pathway of the device scaling, in which the channel materials and their strain configurations, surface orientations and gate stacks are designed specifically for p- and n-FET as illustrated in Fig.2 [7], will offer further opportunities to enhance CMOS device performance. On the other hand, in the high volume manufacturing of LSIs, it should be emphasized that stochastic threshold voltage variation induced by dopant implant position is a great concern. Gate line-edge-roughness is an additional source of variation. These show that accurate dopant position measurement with an atomic scale resolution [8] and extremely precise 3D pattern profiling [9] are needed to model the variations of device characteristics based on the physical parameters.

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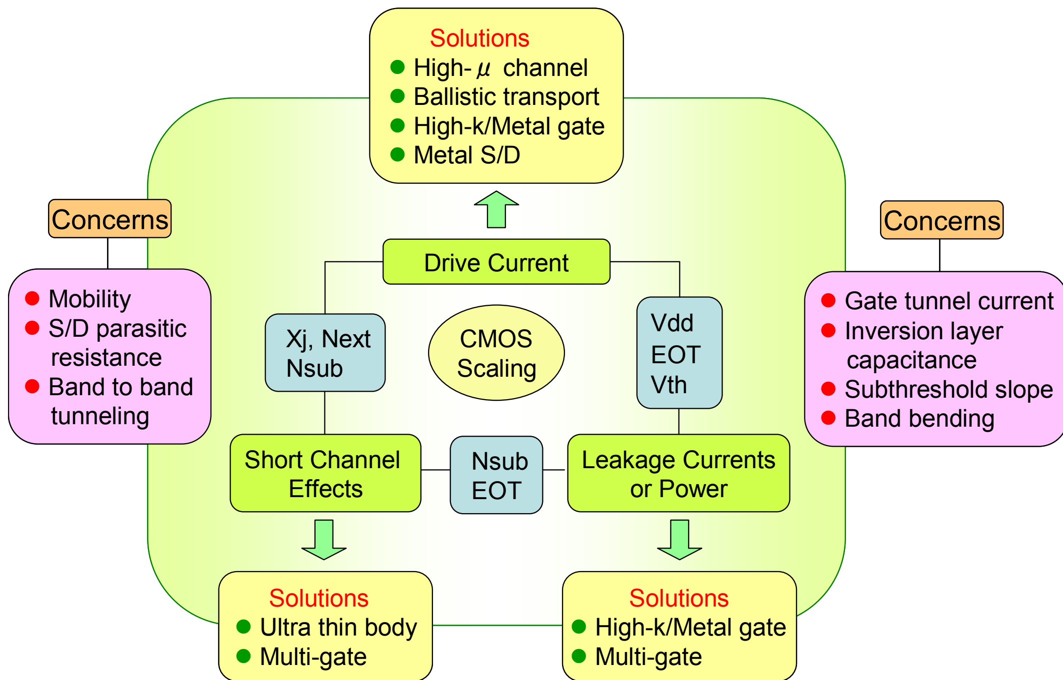

Fig.1 Trade-off factors in device scaling and implementation of new materials and novel structures for enhancing CMOS performance.

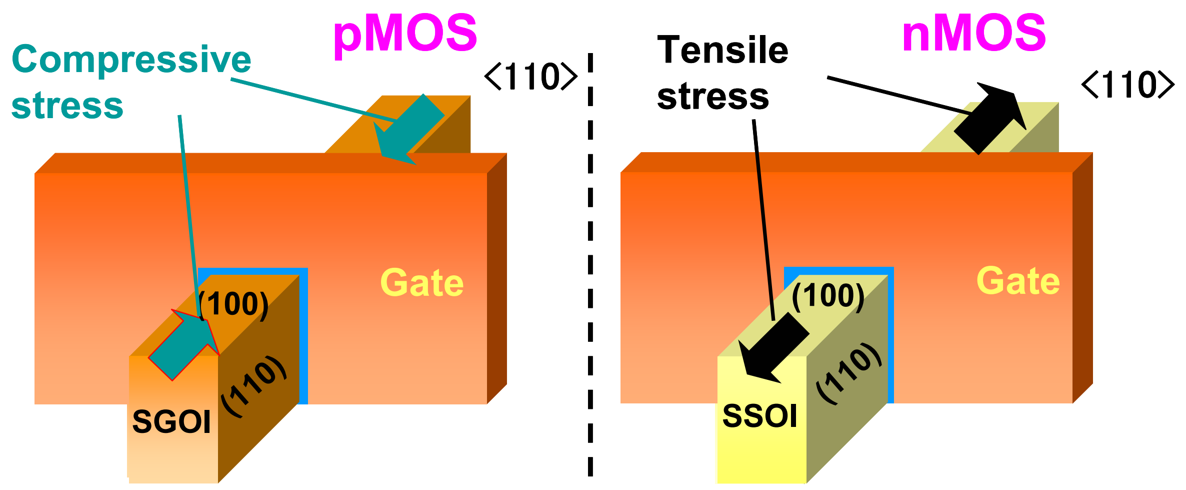

Fig.2 Proposed multi-gate CMOS structures with optimally designed channel-materials, strain-configurations, and surface orientations. SGOI (SiGe on Insulator) pMOS can be integrated with SSOI (Strained Si on Insulator)by using SSOI wafer in combination with local Ge condensation to form SGOI.