Nanoscale Silicon Devices Using Nanostructure Physics for VLSI Applications

Toshiro Hiramoto, Kousuke Miyaji, and Masaharu Kobayashi

Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
hiramoto@nano.iis.u-tokyo.ac.jp

Abstract — This paper describes our recent research work on emerging nanoscale silicon devices using new physical phenomena in nanostructures. It is shown that there are three stages in the research of the silicon nanodevices. Special emphasis will be placed on the first and second stages where new physical phenomena in silicon nanostructures are positively utilized in CMOS-based devices and circuits.

1. Introduction

The silicon MOSFET for VLSI has been scaled down for more than thirty years for higher integration and higher performance. Recently, the miniaturization rate is even accelerated, and the gate length is now less than 40 nm. The silicon devices are certainly in the nanometer regime. Further miniaturization of silicon MOSFETs into nano CMOS will have great impact on the advancement of future information technology. It is predicted in the International Technology Roadmap of Semiconductors (ITRS) [1] that the gate length will become less than 10 nm in 2016 in production. In the research level, a 5 nm CMOS device has already been reported [2]. However, there still are a lot of technical barriers to realize sub-10nm CMOS devices.

The silicon devices will certainly be miniaturized. Then, new physical phenomena, such as quantum effect and single-electron charging effect, will take place even at room temperature in silicon devices. The VLSI device designers have avoided these new physical phenomena in nano-scale structures because these effects sometimes cause unfavorable leakage current and device characteristic fluctuations. However, new physics will definitely take place in future nanodevices. Moreover, new physics have a huge potential for new information processing or data storage, and these new effects in nano-scale structures should be intensively studied and positively utilized for future integrated devices.

In this paper, new physics in silicon nanostructures and potential applications to nanoscale silicon devices are discussed [3].

2. Three Stages of Silicon Nanodevices

Fig. 1 summarizes the future research topics of nanoscale information processing devices. In the author's opinion, there are three stages in silicon nanodevices.

(1) First stage: CMOS extension. The basic operation principle is conventional CMOS, but new physics in nanodevices enhance the performance of nano CMOS.
(2) Second stage: New functions added to CMOS. New function appears in nanodevices by new physics, and the devices are merged into CMOS circuits (still CMOS-based).
(3) Third stage: Beyond CMOS. Nanodevices operate by new physics, and these devices operating by new principle are integrated to form new circuits (not CMOS any more).

Enormous research work has been done and will continue at three stages simultaneously throughout the world. However, the natures of the three stages are very different. Especially, the time scale when the new devices are realized in VLSI products will largely depends on the stage in which these devices are classified. Please note that we are discussing the nanoscale devices for integration, instead of a discrete device. We also focus on the mainstream information processing device technologies including memories, instead of some specific devices for niche applications.

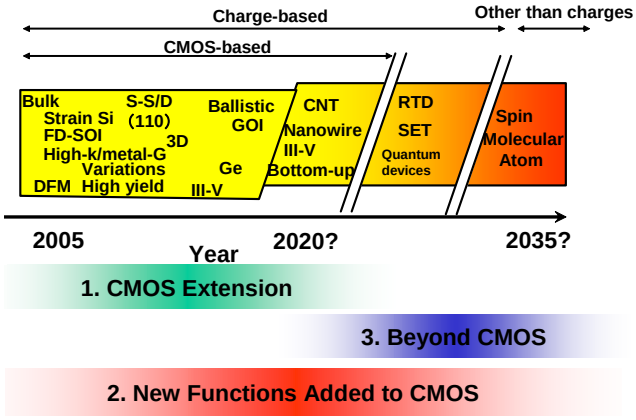

Fig. 1. Future research topics of nanoscale information processing devices and the three stages in the research of nanoscale devices.

The first stage enhances the performance of CMOS by new physics, new structures, and new materials in nanodevices. Since there is no need to change the present CMOS platform for system design and manufacturing, the first stage will come in the nearest future. A paradigm shift

may take place in the middle of the first stage: from the top-down type nanodevices to the bottom-up type nanodevices. If the new fabrication process using, for example, self-assembly that does not depends on lithography is realized, the devices will have higher performance and higher integration level. If the operation principle of a device by the bottom-up process is the same as the conventional CMOS, then this device is classified into the second half of the first stage as shown in Fig. 1.

At the second stage, new devices are merged into CMOS and new functionalities are added. New devices include MEMS devices, sensors, and optical devices. These devices have special features that are not realized in CMOS. Please note that the type of devices that are merged into CMOS will largely depend on applications. The research at the second stage will be driven by application-oriented research. The first stage and the second stage will overlap in time, and they will compete for the developments of future integrated devices. At both the first and second stages, the life of CMOS will be prolonged and they will have great impact on future developments of CMOS and all the information technologies.

At the third stage, however, the circuits are not CMOS any more and completely new types of nanoscale devices, such as spin transistors, will be integrated. Then, the system architecture will not be the same as the conventional one. Therefore, in the present author's opinion, the third stage will be realized as a mainstream device technology only in far future. Although some devices will be realized soon for discrete devices or for applications that are not mainstream technologies, these devices are not discussed in this paper.

3. First Stage: Nano CMOS

When new physics can enhance the performance of CMOS, it will break the performance limit and scaling limit of CMOS. A good example of the first stage is the performance improvement due to quantum confinement effect. The threshold voltage control has been demonstrated experimentally in nanowire channel MOSFETs due to quantum confinement [4]. The higher mobility is also predicted by simulation in nanowire channel MOSFETs [5]. This performance enhancement is scalable, because when the device becomes smaller, more quantum confinement takes place and mobility is more enhanced.

We have experimentally demonstrated the hole mobility enhancement in an ultra-thin FD SOI MOSFET due to quantum confinement [6]. This is one of the best examples of the first stage. Fig. 2 shows a schematic structure of fabricated SOI pMOS devices. The crystal orientation of SOI is (110) and the channel direction is <110>. The SOI thickness is in the range of 3nm. The TEM images of the fabricated devices are also shown in Fig. 2. Fig. 3 shows measured hole mobility as a function of SOI thickness at room temperature. As the SOI becomes thinner, the mobility decreases due to increased acoustic phonon scattering. However, a clear mobility enhancement is observed at 3.4 and 3.6 nm. This phenomenon is explained by the suppression of inter-subband phonon scattering assisted by optical phonon absorption that is the transition between two lowest-lying heavy-hole subbands [6]. Note that the hole mobility increase is observed only in (110) ultra-thin body pMOS, not in (100), due to the high degree of degeneracy of heavy- and light-hole.

Moreover, we have also observed the electron mobility enhancement in a (110) double-gate ultra-thin FD SOI nMOSFET [7]. The mobility enhancement is due to the volume inversion and is observed in the region of high inversion carrier density, where the mobility enhancement is not observed in conventional (100) devices. We have also proposed a FinFET structure with (110) side channel (on conventional (100) substrate) is suitable for CMOS applications [7].

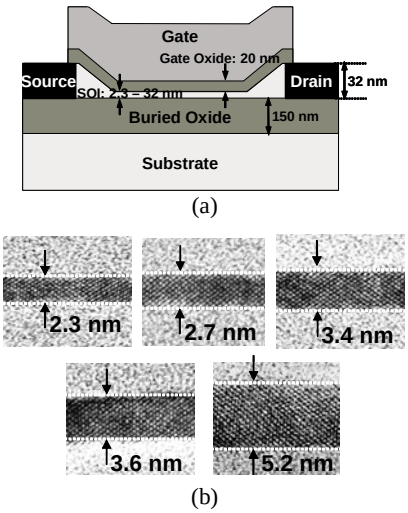

Fig. 2. (a) A schematic of (110)-oriented ultra-thin body SOI pMOS devices. (b) TEM images of measured ultra-thin body pMOS devices.

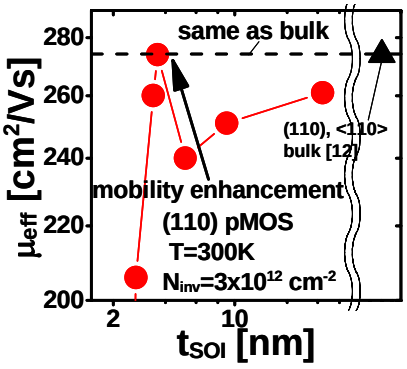

Fig. 3. Measured hole mobility as a function of SOI thickness at room temperature in (110) pMOSFETs.

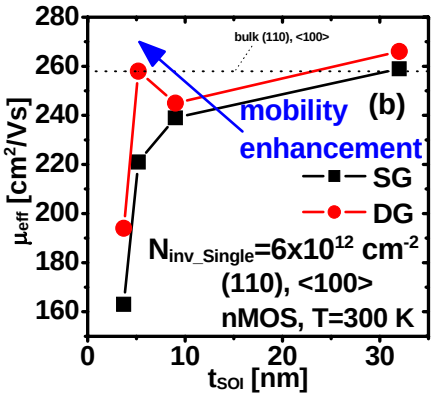

Fig. 4. Measured electron mobility as a function of SOI thickness at room temperature in double-gate (SG) and single-gate (DG) nMOSFETs.

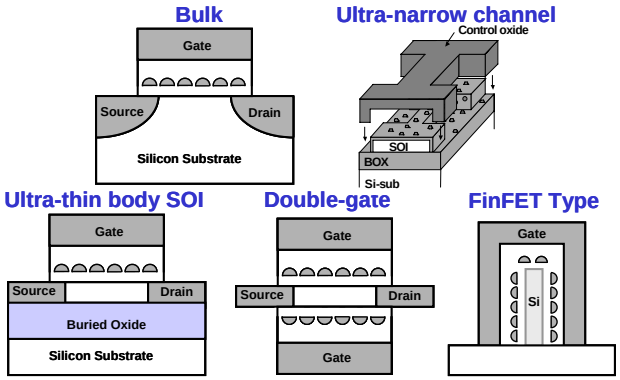

Fig. 5. Silicon nanocrystal memories with different channel structures.

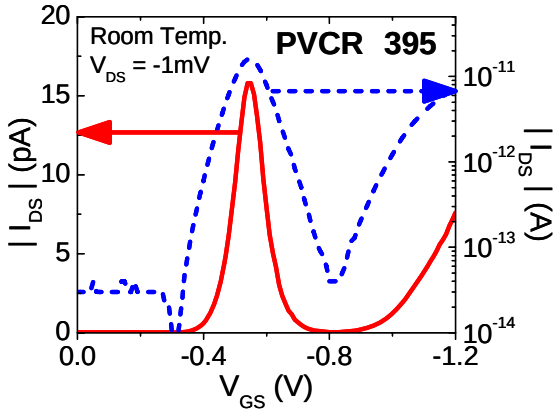

Fig. 6. Coulomb blockade oscillations of a single-hole transistor at room temperature. PVCR is as high as 395.

4. Second Stage: Nanocrystal Memories

The best example of the second stage is a memory. In a new memory device, nano-structures can be adopted only the memory cell and new function can be utilized, while the peripheral circuits are composed of conventional CMOS devices. We have demonstrated a new function in silicon nanocrystal memories, where silicon nanocrystals are embedded in gate oxide and act as charge storages. Physical separation of nanocrystals can improve the retention time by limiting the lateral flow of charges. The new function that appears in silicon nanocrystal memory cell is the two-bit-per-cell operation [8]. The electrons are locally injected only near drain and/or source by hot carrier injection and there are four states depending on where the electrons are injected. Distinct four threshold voltages are experimentally observed that can be read out [8].

We have also investigated the channel structure dependence of memory properties of silicon nanocrystal memory (Fig. 5). The enhancement of memory window and retention time has been observed in double-gate and FinFET type channel due to the interactions of electrons in both gate electrodes.

5. Second Stage: Analog Applications of SETs

A single-electron transistor (SET) is one of the most well known nanodevices and is recognized as a basic device element for future ultra-low power integrated circuits. Although many circuit applications of SETs have been proposed so far, these applications are classified into the third stage where new devices operating new principle are integrated to form new circuits. If SET is in the second stage, there is more potential to be realized as a new functional device in near future. Here, a new application of SET in the second stage is shown.

Our single-electron/hole transistors are in the form of a point contact MOSFET. The silicon quantum dot is naturally formed in the very narrow channel and the device acts as a single-electron/hole transistor [9]. Great efforts have been made to raise the operation temperature. Fig. 6 shows I-V characteristics at room temperature [10]. Recently, we observed even larger Coulomb blockade oscillations with peak-to-valley current ratio (PVCR) of 480, which is the largest oscillations in a single-dot system ever reported [11]. The estimated dot size is as small as 2nm.

Then, further great efforts have been made to integrate room-temperature operating single-electron/hole transistor. Fig. 7 shows Coulomb blockade oscillations of three integrated single-hole transistors on a chip [12]. This is the first integration of the room-temperature operating single-electron/hole transistors. Moreover, each single-hole transistor has silicon nanocrystals embedded in the gate oxide and acts as a non-volatile memory. Therefore, the peak position of Coulomb blockade oscillations can be controlled by programming [12].

The bell-shaped I-V characteristics can be utilized for the analog pattern matching circuits [13]. The Coulomb blockade oscillations have certainly the bell-shaped I-V characteristics, so we apply them to the analog pattern

matching. In this application, the matching is performed by the single-hole transistors and other calculations are done by CMOS circuits. Therefore, this is a new architecture utilizing single electron/hole transistors in the second stage.

The three integrated single-hole transistors shown in Fig. 7 correspond to three elements of a vector. For simplicity, the three elements are fitted to the three basic elements of colors (RGB). Then, color "orange" is stored by programming and various other colors are input. The results are shown in Fig. 8. Largest current is clearly obtained by input of "orange", indicating that "orange" is successfully read out [12].

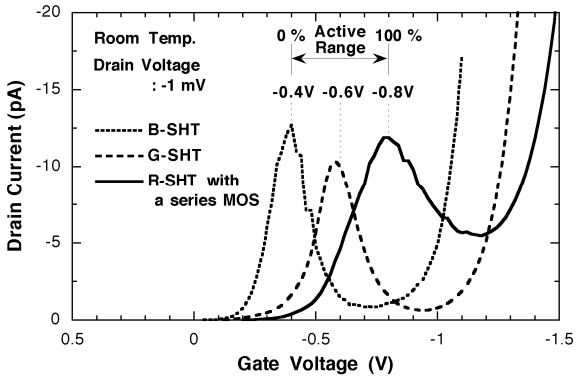

Fig. 7. I-V characteristics of integrated three single-hole transistors operating at room temperature. "Orange" is stored by shifting the peak positions by programming.

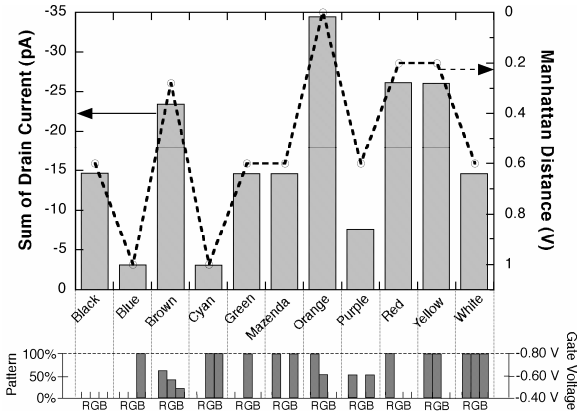

Fig. 8. Measured total current of three integrated single-hole transistors. "Orange" is successfully read out.

7. Conclusion

Our recent work on silicon nanodevices is presented. It is shown that there are three stages in the nanoscale silicon devices and that the positive utilization of new physics in nano-structures will be essential. These new technologies will break the performance and scaling limit of CMOS, and CMOS will continue to be a mainstream device for VLSI.

Acknowledgment

This work was partly supported by Grant-in-Aid for COE Research, Scientific Research, and the IT program from MEXT, Japan.

References

[1] International Technology Roadmap of Semiconductors (ITRS) (http://public.itrs.net/).

[2] H. Wakabayashi et al., "Sub-10-nm Planar-Bulk-CMOS Devices using Lateral Junction Control", Technical Digests of International Electron Devices Meeting (IEDM), pp. 989 – 991, 2003.

[3] T. Hiramoto, M. Saitoh, and G. Tsutsui, "Emerging nanoscale silicon devices taking advantage of nanostructure physics", IBM Journal of Research and Development, Vol. 50, No. 4/5, pp. 411 – 418, July/September, 2006.

[4] H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental Evidence for Quantum Mechanical Narrow Channel Effect in Ultra-Narrow MOSFETs", IEEE Electron Device Letters, Vol. 21, No. 8, pp. 396 - 398, August, 2000.

[5] H. Majima, Y. Saito, and T. Hiramoto, "Impact of quantum mechanical effects on design of nano-scale narrow channel n- and p-type MOSFETs", Tech. Dig. International Electron Devices Meeting (IEDM), pp. 733 – 736, 2001.

[6] G. Tsutsui, M. Saitoh, and T. Hiramoto, "Experimental Study on Superior Mobility in (110)-Oriented UTB SOI pMOSFETs", IEEE Electron Devices Letters, Vol. 26, No. 11, pp. 836 – 838, 2005.

[7] G. Tsutsui, M. Saitoh, T. Saraya, T. Nagumo, and T. Hiramoto, "Mobility Enhancement due to Volume Inversion in (110)-oriented Ultra-thin Body Double-gate nMOSFETs with Body Thickness less than 5 nm", International Electron Devices Meeting (IEDM), pp. 747 - 750, December, 2005.

[8] I. Kim, K. Yanagidaira, and T. Hiramoto, "Scaling of Nano-Crystal Memory Cell by Direct Tungsten Bitline on Self-Aligned Landing Plug Polysilicon Contact", IEEE Electron Devices Letters, Vol. 25, No. 5, pp. 265 – 267, 2004.

[9] M. Saitoh and T. Hiramoto, "Extension of Coulomb Blockade Region by Quantum Confinement in the Ultrasmall Silicon Dot in a Single-Hole Transistor at Room Temperature", Applied Physics Letters, Vol. 84, No. 16, pp.3172 – 3174, 2004.

[10] K. Miyaji, M. Saitoh, and T. Hiramoto, "Voltage gain dependence of the negative differential conductance width in silicon single-hole transistors", Applied Physics Letters, Vol. 88, No. 14, 143505, 2006.

[11] M. Kobayashi and T. Hiramoto, "Experimental Study on Quantum Structure of Silicon Nano Wire and Its Impact on Nano Wire MOSFET and Single-Electron Transistor", IEEE International Electron Devices Meeting (IEDM), .pp. 1007 – 1009, 2006.

[12] M. Saitoh, H. Harata, and T. Hiramoto, "Room-Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching", IEEE Electron Devices Meeting (IEDM), pp. 187 – 190, 2004.

[13] T. Yamasaki and T. Shibata, IEEE Trans. on Neural Networks, Vol. 14, p. 1257, 2003.