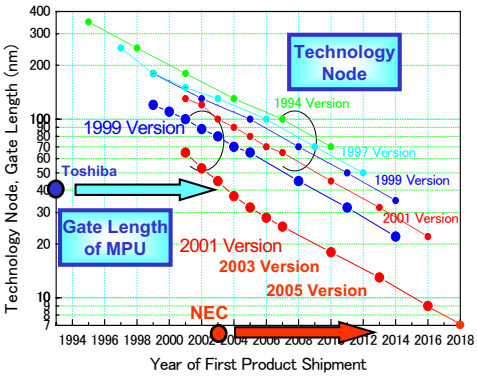
Nanoscale Silicon Devices Using Nanostructure Physics for VLSI Applications

T. Hiramoto, K. Miyaji, M. Kobayashi
Institute of Industrial Science, University of Tokyo
hiramoto@nano.iis.u-tokyo.ac.jp

1. Introduction: Three stages in Silicon Nanoelectronics
2. The First Stage: Mobility Enhancement
3. The Second Stage
   3.1. Silicon Nanocrystal Memories
   3.2. Single-Electron Transistors
4. Summary

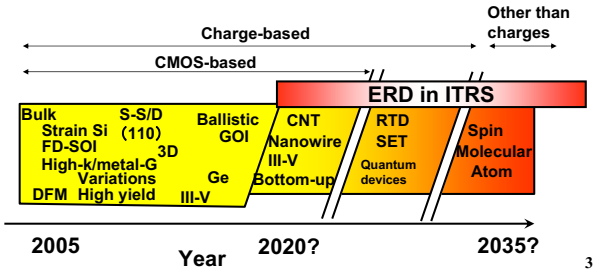
ITRS (Roadmap)



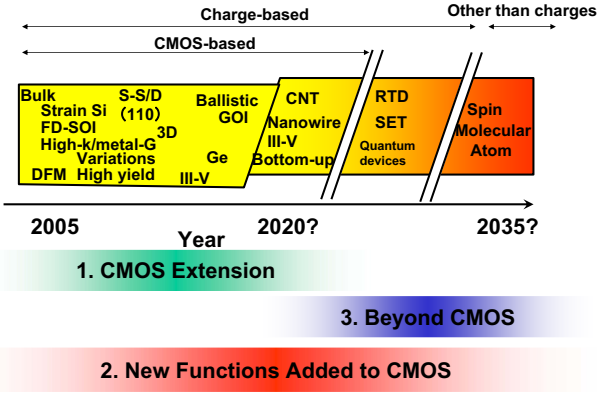
Transistors (Information Processing)

Information Processing Devices

- No better device other than CMOS in "charge-based". CMOS extension will be the most important.
- CNT-FET will also be classified to "CMOS Extension".



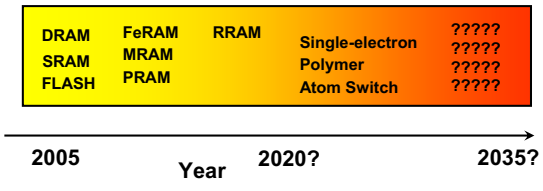
Three Stages in Silicon Nanoelectronics



Memories

Memory and Storage Devices

- New materials and nano-structures only for memory cells
  Other circuits are based on conventional CMOS
- Good examples of the second stage

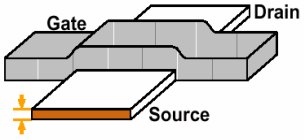


2. The First Stage – CMOS Extension

Mobility Enhancement by Quantum Confinement

Quantum Confinement

Thin Channel (SOI MOSFET)

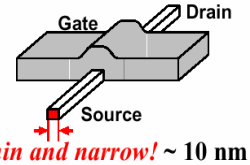


thin but wide

Only vertical confinement
No horizontal confinement

Threshold voltage depends on **SOI thickness**

Thin and Narrow Channel (Ultra-Narrow MOSFET)

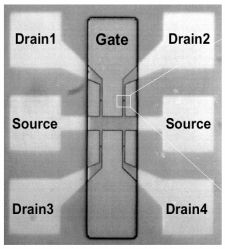


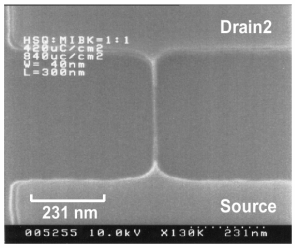
thin and narrow! ~ 10 nm

Vertical and horizontal confinement

Threshold voltage depends on **channel width**

SEM Images of Ultra-Narrow Channels

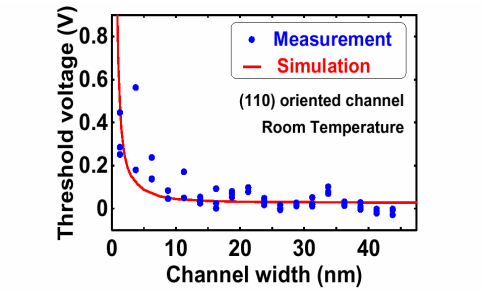




Channel width	< 10 nm
Channel length	250 nm
Gate oxide thickness	34 nm
SOI thickness	7 nm

H. Majima et al., IEDM, 1999.

Threshold Voltage Increase

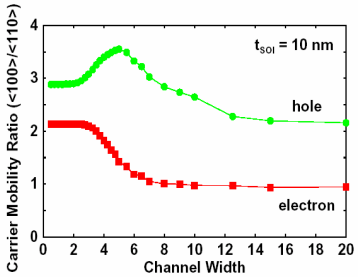


The threshold voltage increase is caused by the quantum narrow channel effect.

H. Majima, IEDM, p.379, 1999.
H. Majima et al. IEEE EDL, 21, 396 (2000).

Higher Mobility in [100] Direction

Electron and hole mobility ratio between <100> and <110> ultra-narrow MOSFET

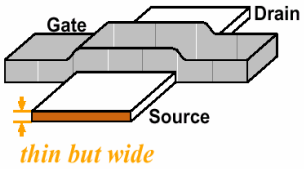


<100> mobility higher

H. Majima et al. IEDM, 2001.

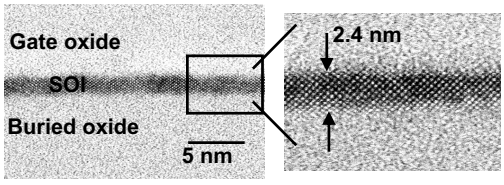
Higher electron and hole mobility is found in <100> ultra-narrow MOSFET.

2-D: Ultra-Thin Channel

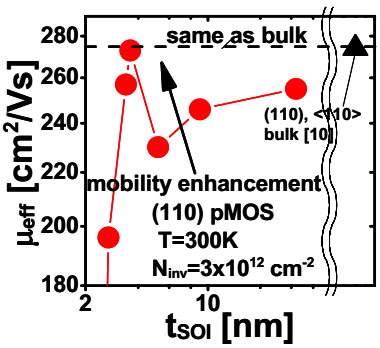


thin but wide

- (110) PMOS and NMOS
- t_{OX}: 20nm
- t_{BOX}: 150nm
- t_{SOI}: 2.3 – 32nm
- L_g/W_g: 200μm/200μm
- <110> directed channel



Mobility Enhancement in (110) PMOS

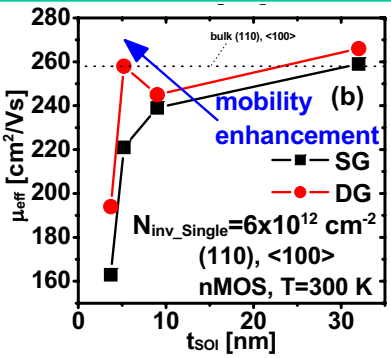


- N_{inv} = 3x10^{12} cm^{-2}
- Mobility at 3.6nm is as high as bulk PMOS
- Suppression of inter-subband phonon scattering assisted by optical phonon absorption that is the transition between two lowest-lying heavy-hole subbands

G. Tsutsui et al., VLSI Technology Symposium, p.76, 2005.

[10] H. Irie et al., IEDM, 2004, p.225.

Mobility Enhancement in (110) NMOS



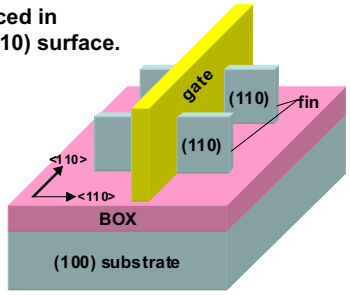
- N_{inv} = 6x10^{12} cm^{-2}
- No enhancement in single-gate NMOS
- Mobility enhancement due to volume inversion in (110) NMOS at t_{SOI} = 4nm.

G. Tsutsui et al. IEDM, p. 747, 2005. 13

(110) CMOS

- pMOS is the best in a (110) surface.
- nMOS mobility is enhanced in double-gate channel in (110) surface.

- FinFET in a (100)-oriented substrate.



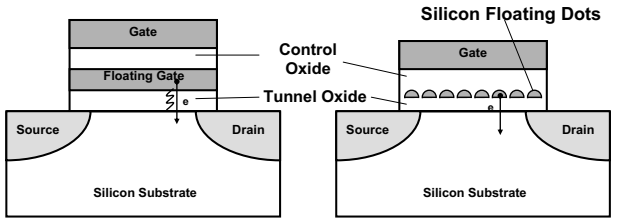
G. Tsutsui et al. IEDM, p. 747, 2005. 14

3. The Second Stage – New Functions Added to CMOS

3.1. Silicon Nanocrystal Memories

15

Comparison with Flash Memory

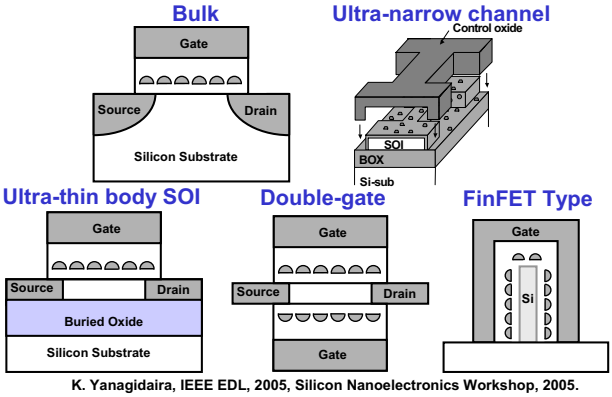


Flash Memory | Silicon Nanocrystal Memory

- Proposed by Prof. S. Tiwari
- Higher endurance and higher reliability
- Tunnel oxide can be thin
  - ⇒ Lower voltage operation, lower power and higher speed
  - ⇒ Scalable

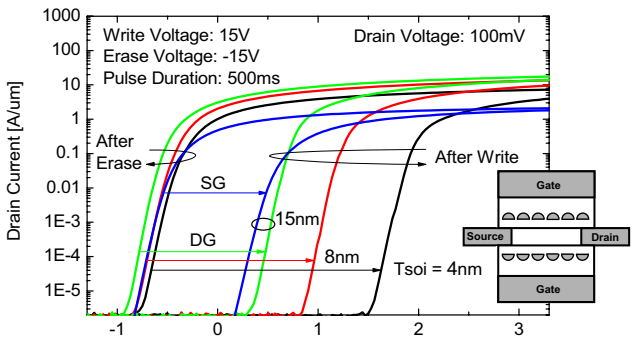
16

Modification of Channel Structures



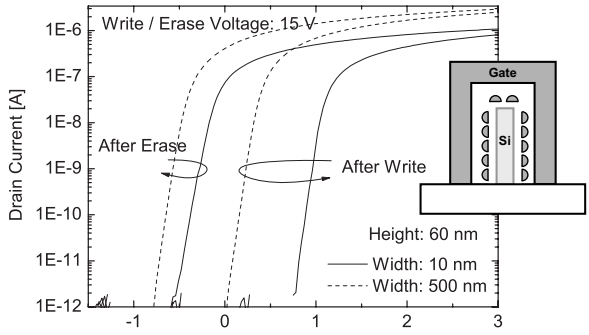
K. Yanagidaira, IEEE EDL, 2005, Silicon Nanoelectronics Workshop, 2005. 17

Double-Gate Nanocrystal Memory



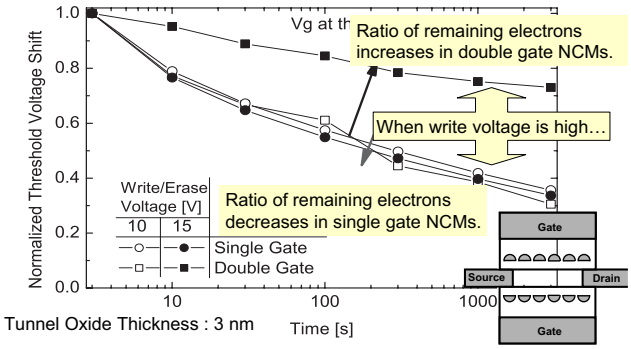
K. Yanagidaira et al, IEEE EDL, vol. 26, p. 473, 2005. 18

FinFET-Type Nanocrystal Memory



Tunnel Oxide Thickness : 3 nm
Control Oxide Thickness: 30 nm

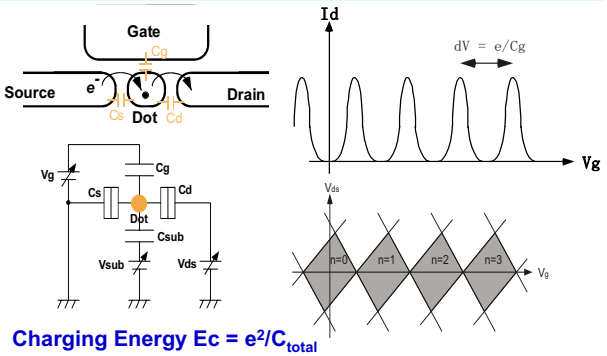
Retention Time Improvement



Tunnel Oxide Thickness : 3 nm

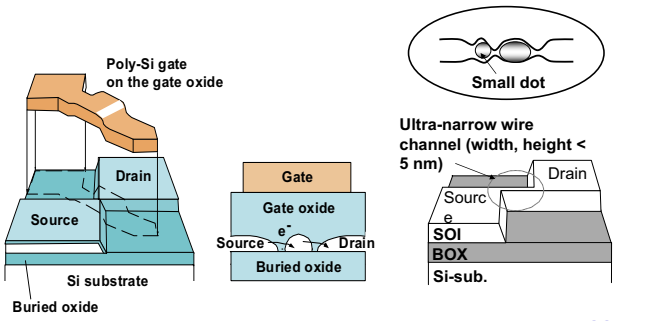
3.2. Single-Electron Transistor (SET)

Single-Electron Transistor



Charging Energy $Ec = e^2/C_{total}$
Temperature $T < Ec$ (Ec ~ 26 meV when d ~ 10 nm)

Fabrication of Single-Electron Transistor

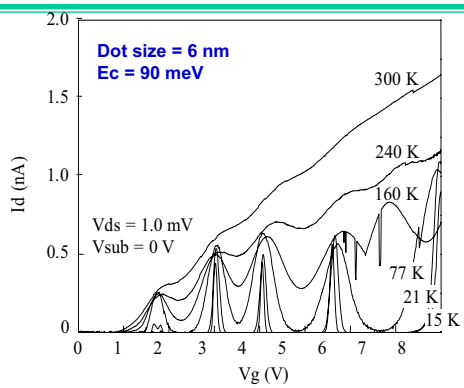


Point Contact MOSFET

Ultra-narrow channel MOSFET

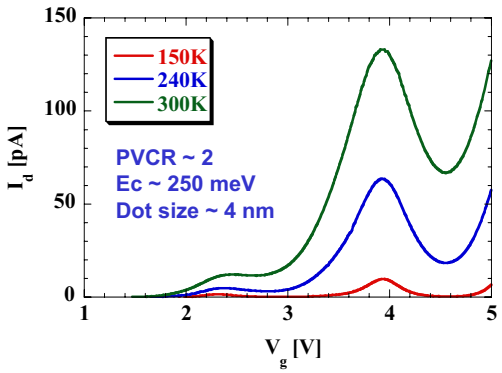
**H. Ishikuro and T. Hiramoto, *Appl. Phys. Lett.* 74 (1999) 1126.

Coulomb Blockade Oscillations



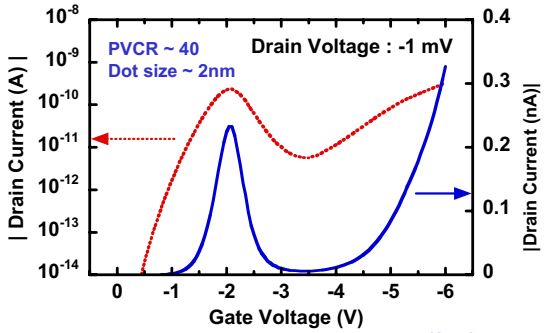
H. Ishikuro and T. Hiramoto, Appl. Phys. Lett. 71, 3691, 1997.

Large Oscillations at Room Temperature



M. Saitoh et al., Jpn. J. Appl. Phys. 40, 2010 (2001). 25

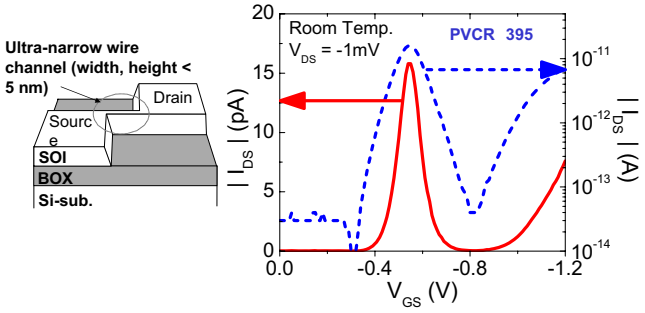
Coulomb Blockade Oscillations at RT



A p-type device: a single-hole transistor (SHT)

M. Saitoh and T. Hiramoto, IEDM, p. 753, 2003
M. Saitoh and T. Hiramoto, Appl. Phys. Lett. 84 (2004) 3172 26

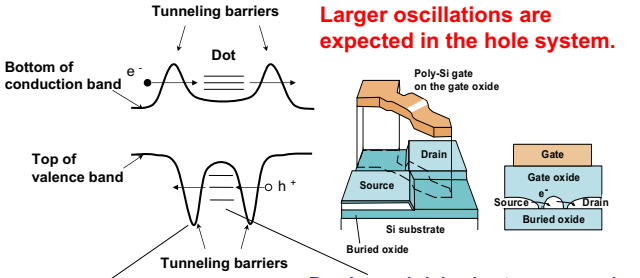
Largest CB Oscillations at RT



Largest CB Oscillations at room temperature!

K. Miyaji et al. , Applied Physics Letters, 143505, 2006. 27

Possible Formation Mechanism of a Dot



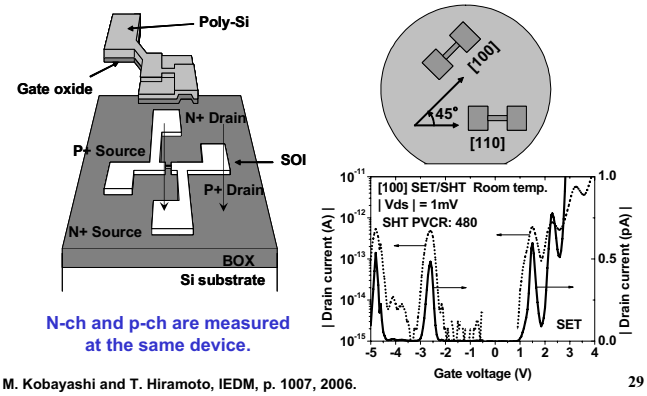
Larger oscillations are expected in the hole system.

Band gap shrinks due to compressive strain by thermal oxidation*

Band gap expands by quantum confinement**

*K. Shiraishi et al. *Physica E* 7 (2000) 337.
**H. Ishikuro and T. Hiramoto, *Appl. Phys. Lett.* 74 (1999) 1126. 28

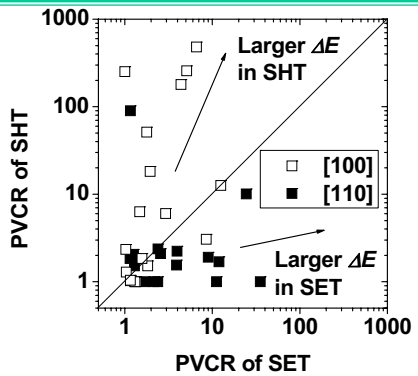
Charge Polarity and Direction Dependence



N-ch and p-ch are measured at the same device.

M. Kobayashi and T. Hiramoto, IEDM, p. 1007, 2006. 29

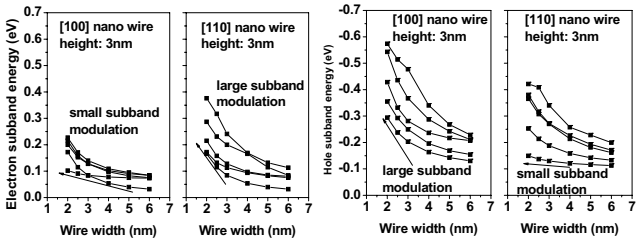
Comparison of SET and SHT



M. Kobayashi and T. Hiramoto, IEDM, p. 1007, 2006. 30

Quantum Confinement Energy

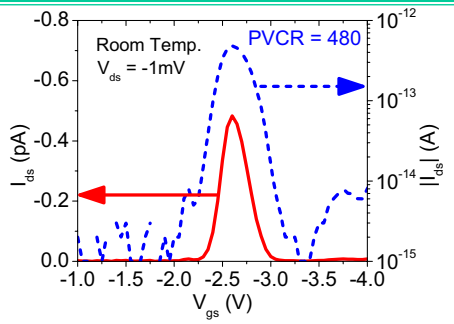
Simulation



Electrons Holes

M. Kobayashi and T. Hiramoto, IEDM, p. 1007, 2006. 31

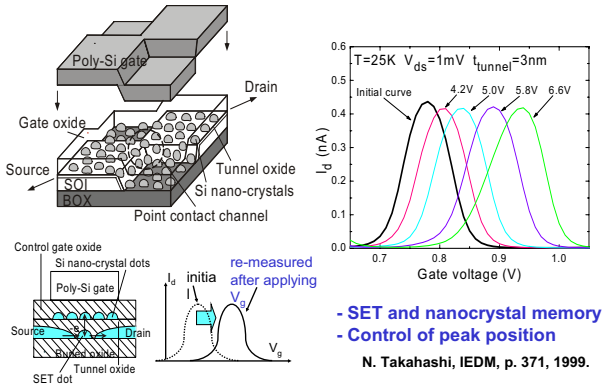
Even Larger CB Oscillations



Quantum Confinement Effect depends on Direction and Charge Polarity. [100]/(100) PMOS has the largest oscillations.

M. Kobayashi and T. Hiramoto, IEDM, p. 1007, 2006. 32

More Functionality (Data Storage)

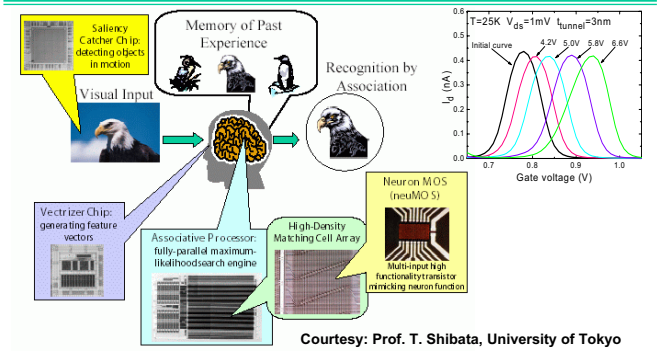


- SET and nanocrystal memory
- Control of peak position

N. Takahashi, IEDM, p. 371, 1999.

33

Application to Analog Pattern Matching



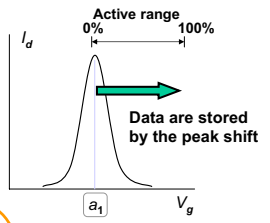
Courtesy: Prof. T. Shibata, University of Tokyo

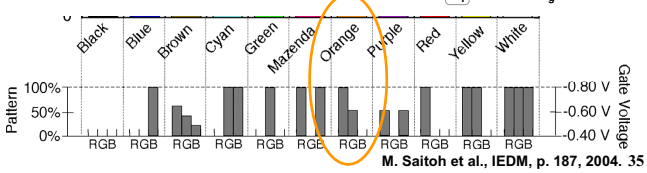
The input image and storage data are compared in pattern matching. The 2D data are translated into 1D data to simplify the processing.

34

Storage of Colors and Read

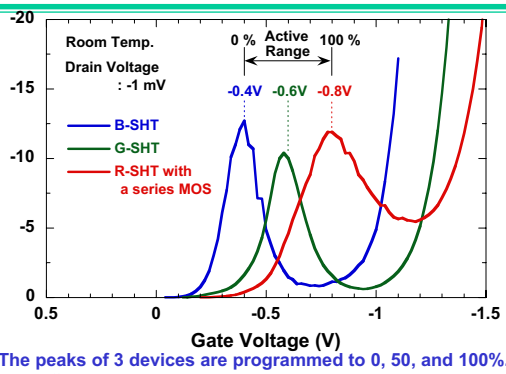
- Three SHTs operating at RT are integrated in one chip.
- Pattern matching of 3-element vector: each SHT corresponds to RGB and a color is stored and is read.
- "Orange" is stored.





M. Saitoh et al., IEDM, p. 187, 2004. 35

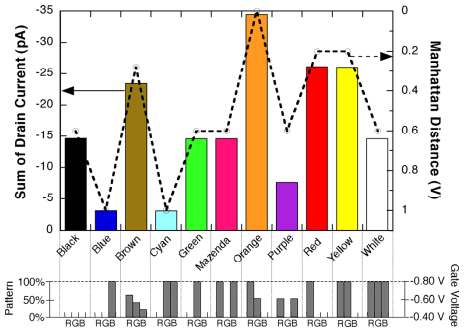
After Writing



The peaks of 3 devices are programmed to 0, 50, and 100%. Then, "orange" are stored in memory.

M. Saitoh et al., IEDM, p. 187, 2004. 36

Reading (Sum of the Current)



The output current reflects the similarity between input and "orange".
The output is the largest when "orange" is input.

M. Saitoh et al., IEDM, p. 187, 2004.

Summary

1. There are three stages in the research of silicon Nanoelectronics.
2. "CMOS Extension" and "New Functions Added to CMOS" will be important.
3. Mobility enhancement by quantum confinement.
4. SETs/SHTs should be merged into CMOS.