Characterization of Electronic Charged States of Si-based Quantum Dots for Multi-valued MOS Memories

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Abstract

For Si dots individually charged with a few electrons or holes, characteristic potential profiles with a dimple around the center of the charged Si dot are observed and can be interpreted in terms of the Coulomb repulsion among the charges retained in the dot. By an introduction of Ge core in Si dots, holes can be well-confined in the Ge core while electrons are stored in the Si clad because of the energy band discontinuity at the interface between the Si clad and the Ge core. The influence of ionized impurity doping to Si-QDs on their electron charging and discharging characteristics has also been studied. For metal-oxide-semiconductor (MOS) capacitors and n-channel MOS field-effect-transistors (n-MOSFETs) with Si-QDs floating gates, distinct multiple-step charging to (or discharging from) the Si-QDs floating gate have been confirmed at room temperature, which are regulated presumably by redistribution of injected electrons in the Si-QDs floating gate for further electron injection (or emission).

1. Introduction

The application of Si-QDs to floating gate MOS memories has attracted increasing attention because of its feasible advantage for multi-valued operations in addition to practical advantages in charge retention and endurance characteristics compared to conventional planer floating gate memories [1-4]. The control of discrete charged states of the Si-QDs floating gate is a key to achieve distinct multi-valued operations at room temperature and above. Considering that charging energy and quantization energy of each dot in each Si-QD are strongly size dependent, the size uniformity of Si-QDs with an areal density comparable to the channel electron density is a crucial factor. In that regard, the self-assembling process is thought to be adequate to control the formation of high density Si-QDs on SiO_2.

In our previous work, we have demonstrated spontaneous formation of Si-QDs on thermally-grown SiO_2 with a fairly uniform size distribution and a high areal density ($>10^{11}cm^{-2}$) by controlling the early stage of LPCVD from SiH_4 [5], and demonstrated unique multiple-step electron charging in the Si-QDs floating gate even at room temperature [6, 7]. For precise control of the multi-valued memory operation, a clear insight into the charging and discharging characteristics of the Si-QDs is imperative.

In this paper, our recent results on the characterization of electronic charged states of Si-QDs with and without Ge core are reviewed, and the impact of impurity doping to Si-QDs on their charged states is demonstrated. Also, from multi-step electron charging and discharging characteristics of the Si-QDs floating gate, we show that the Coulomb interaction among electrons in neighboring charged QDs and in channel plays an important role into the characteristic progress of charge distribution in the Si-QDs floating gate.

2. Evaluation of Electronic Charged States of Individual Si QD with and without Ge core

We reported that, for Si dots with core heights in the range from 6 to 12nm on ~4nm-thick SiO_2/p-Si(100), the potential changes caused by single electron injection and emission were detected by the non-contact AFM/Kelvin probe technique [8]. We have extended our research to characterize electronic charged states of bigger Si dots with and without Ge core, in which a few electrons or holes can be stably retained [9]. For the evaluation of the charged states of individual dots, the dot formation was controlled so that the areal dot density was as low as $\sim 10^8 cm^{-2}$, where the mean distance among the dots was sufficiently larger than a lateral resolution of the Kelvin probe method used in this study. Before and after scanning an electrically-biased Au- or Rh-coated AFM tip on the sample surface in a tapping mode, the topographic images and corresponding surface potential images were simultaneously taken in the non-contact Kelvin probe mode. A series of these experiments was preformed under clean room air at room temperature. After electron injection to and extraction from Si dots larger than 20nm in height, unique surface potential images having a dimple around the center of the charged dots are observed (Fig. 1). Considering the capacitance between the Si dot and the substrate, it is found that the observed surface potential changes are caused by a few electrons or holes retained in the dot. Thus, the observed dimpled potential image is attributable to columbic repulsion force among charges in the Si dot. In fact, the dimpled surface potential change diminishes with time due to the progressive emission of retained electrons to the Si substrate. In the Si dots with Ge core [10], the surface potential image after electron injection shows a clear dimpled potential profile in the center of the dot, but in contrast, the maximum potential change appears in the center of the dot after hole

injection (Fig. 2). These results imply that injected electrons and holes are located in the Si clad and the Ge core, respectively, as suggested from the type II energy band discontinuity [11] between Si and Ge.

The influence of impurity doping to Si-QDs on their electron charging and discharging characteristics has also been studied [12]. P-doped or B-doped Si-QDs were prepared by a pulse injection of 1% PH_3 or B_2H_6 diluted with He during the dot formation on thermally-grown SiO_2 from thermal decomposition of pure SiH_4. It is found that the tip biases required for electron injection to and emission from the dots are changed by doping as shown in Fig. 3. The potential change caused by the extraction of one electron was observed after applying a tip bias as low as +0.2V for P-doped Si dots while, for undoped and B-doped Si dots with almost the same size as the P-doped Si dot, no such a surface potential change was detectable at tip biases of not less than +1V. On the other hand, the injection of one electron to the B-doped Si dot was occurred at a tip bias as low as -0.2V although the electron injection to undoped and P-doped Si dots requires much negative tip biases over -1.0 V. The results indicate the electron extraction from the conduction band of the P-doped Si dot and the electron injection to the valence band of the B-doped Si dot, which elicit a positively-ionized P donor and a negatively-ionized B acceptor, respectively.

3. Characteristics of MOS Capacitors with Si-QDs as a Floating Gate

We have studied electron charging and discharging characteristics of Si-QDs as a floating gate of Al-gate MOS capacitors and so far demonstrated unique hysteresis characteristics in high-frequency capacitance-voltage (C-V) and displacement current-voltage (I-V) curves measured at room temperature in dark. The

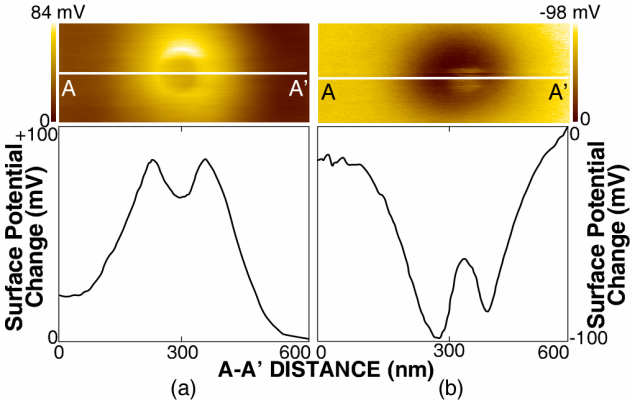

Fig. 1 The surface potential images and profiles across the Si dots after (a) electron emission at a tip bias of +3V and (b) electron injection at -3V. The dot heights and the estimated retained charges are 21nm and 4 holes for (a) and 25nm and 5 electrons for (b), respectively.

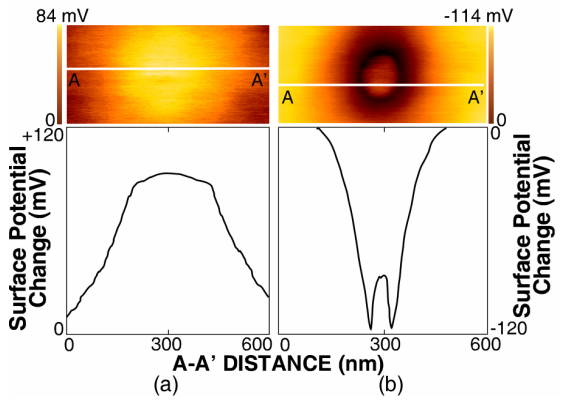

Fig. 2 The surface potential images and profiles across the Si dots with a Ge core after (a) electron emission and (b) electron injection. The dot heights and the estimated retained charges are 16.2nm and 2-3 holes for (a) and 20nm and 3 electrons for (b), respectively.

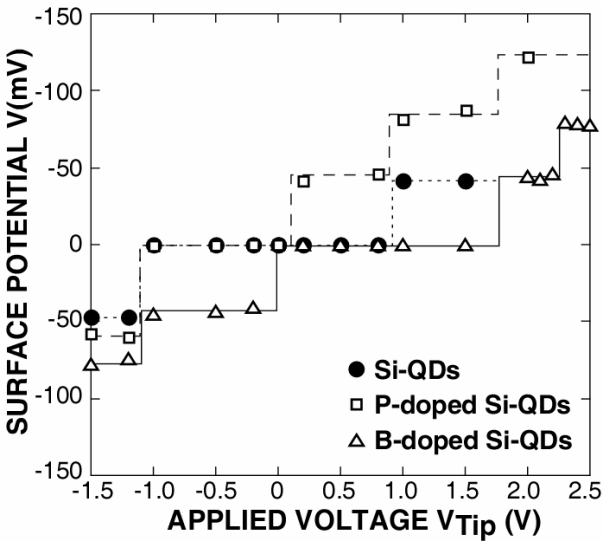

Fig. 3 The surface potential changes for undoped, P-doped and B-doped Si dots with ~6nm in height as functions of tip bias.

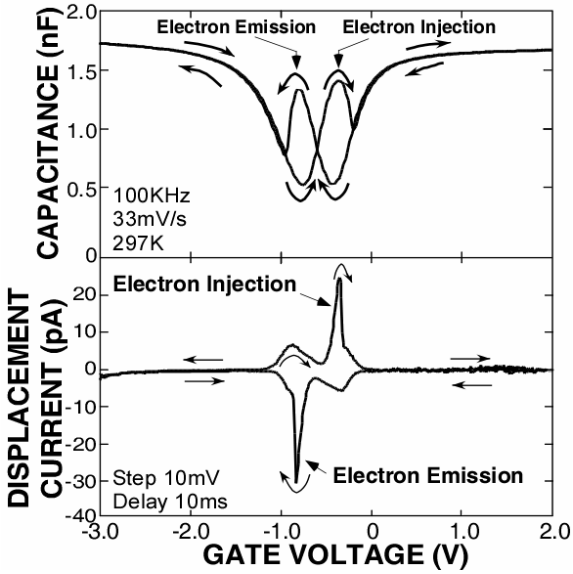

Fig. 4 100kHz C-V and displacement I-V characteristics of an Al-gate MOS capacitor with a Si-QDs floating gate measured at room temperature and under cold light illumination.

hysteresis characteristics show a symmetrical pattern reflecting the Fermi energy of the substrate and both the capacitance and displacement current peaks appear around the flat-band condition. Thus, one can rule out the contribution of traps to the measured hysterisis characteristics.

For the evaluation of charged states of the Si-QDs floating gate under inversion conditions, cold light irradiation in the wavelength region of 400-800nm was carried out during high-frequency C-V and I-V measurements [13], where photo-generated carriers in the vicinity of the area masked with the Al gate flow into beneath the gate oxide and respond to the gate voltage modulation even at a high frequency. As typically shown in Fig.4, in the C-V curve measured by scanning the gate voltage from -3V toward the positive side, a distinct capacitance peak due to the electron injection to the Si-QDs floating gate from the inverted substrate observed at -0.3V by the light irradiation. On the other hand, in the C-V curve measured by scanning backward from +2V, a similar capacitance peak but due to the electron emission from the Si-QDs floating gate to the substrate, being identically seen in dark, was observed at -0.8V. In addition, the displacement current shows a marked positive peak due to the transition from the electrically neutral state to the charged state and an equivalent negative peak due to the opposite transition. Subsidiary displacement current components are attributed to electron injection and emission in the depletion conditions. In the strong inversion and accumulation conditions, the displacement current was hardly observed because the electron concentration of the Si surface was changed within the delay time.

4. Characterization of Multistep Charging to Si-QDs Floating Gate in n-MOSFETs

We have fabricated n-MOSFETs with a doubly-stacked Si-QDs floating gate [6, 7], and confirmed the multi-step electron charging to the Si-QDs floating gate associated with Coulomb blockade effect from distinct bumps in drain current-gate voltage characteristics observed in ramping up the gate voltage after complete discharging at room temperature. We have also found that, in the temporal change in the drain current at a constant gate bias, Id-t, the electron injection to the Si-QDs floating gate proceeds stepwise through metastable states with a fairly long incubation period to the next charging (Fig. 5) and is accelerated by temperature and visible light irradiation as well as gate bias [15-17]. A decrease in the drain current level is a good indicator of an increase in the number of electrons injected into the Si-QDs floating gate. During the metastable state where the number of electrons in the floating gate is almost unchanged, injected electrons are likely to be redistributed in the Si-QDs floating gate to trigger further electron injection. In fact, when the gate voltage is switched to zero bias in the early stages of a metastable state, a temporal increase in drain current attributable to the electron emission is observed but with spending time in the metastable state, it becomes hardly observable [17]. From the temperature dependence of Id-t characteristics, it is also found that the electron charging in dark proceeds with an activation energy corresponding to the 1st and 2nd energy states in neighboring dots.

To gain a better understanding of the charging characteristics of the Si-QDs floating gate, the temporal change in the drain current after applying positive pulsed gate biases have been measured systematically as functions of pulse voltage height and width [18]. The electron charging with pulsed gate biases below certain height and width can not create a metastable state. As shown in Fig. 6, after the positive gate pulse below 1.25V or below 0.95s, the drain current measured at zero gate bias increases temporarily to some current level reflecting the electron emission from the Si-QDs floating gate and in a little while decreases significantly down to the current level for the metastable charged state. Notice that an increase in the pulse height only by 10mV

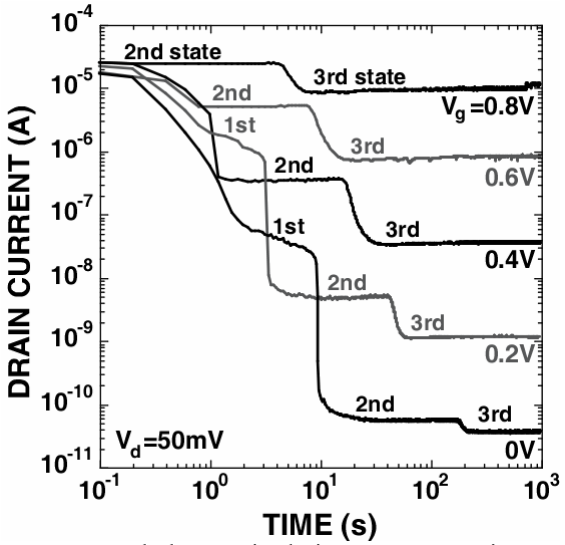

Fig. 5 Temporal changes in drain current at various gate biases after complete discharging at a gate bias of -4V.

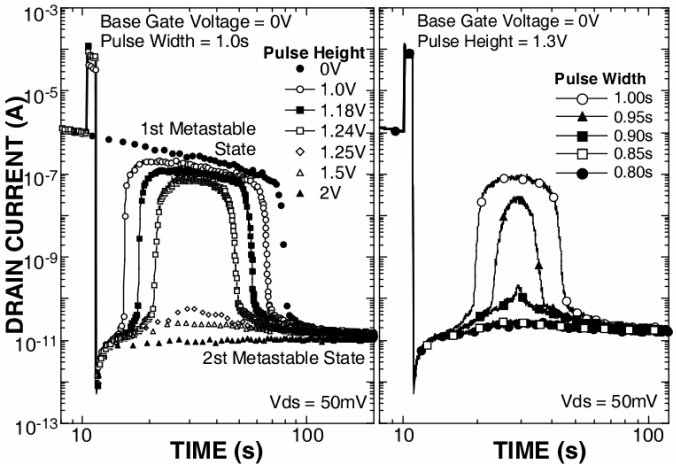

Fig. 6 Temporal changes in drain current at gate voltage of 0V after applying pulse gate biases (a) with different pulse heights at a constant pulse width of 1s and (b) with different pulse widths at a constant pulse height of 1.3V.

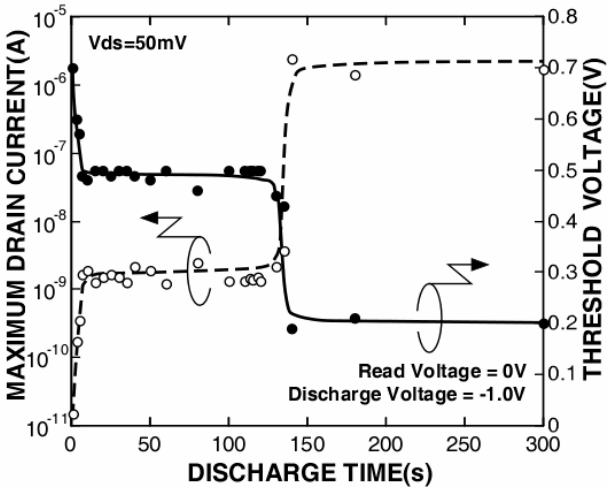

Fig. 7 The maximum drain currents and corresponding threshold voltages as functions of discharge time.

from 1.24V or in the pulse width by 50ms from 0.9s can generate a metastable charged state. The results indicate that the pulse height and width are crucial factors to realize the charge distribution for a stable charged state.

Discharging characteristics of Si-QDs floating gate have also studied in the following method [19, 20]. After being fully charged at +3V, the Si-QDs floating gate was discharged for a length of time at a certain negative V_G and then gate voltage was switched to 0V to monitor the progress in the discharging of the Si-QDs floating gate. By switching the gate voltage to 0V, the drain current was increased immediately and then decreased due to the electron charging to the Si-QDs floating gate. The maximum drain current measured after switching to 0V was plotted as a function of discharging time as shown in Fig. 7. Obviously, the maximum drain current increases stepwise so that the discharging of the Si-QDs floating gate proceeds throughout an intermediate charged state. In the intermediate state, since the maximum drain current is almost constant with respect to discharging time, the amount of charge in the Si-QDs floating gate remains unchanged. This result suggests the change in electron distribution in the Si-QDs floating gate during the intermediate state as in the case of electron charging.

5. Summary

For Si-QDs charged with a few electrons or holes, surface potential images show a characteristic potential profile with a dimple around the center of the charged dots, being interpreted in terms of the Coulomb repulsion among the charges retained in the dot. By an introduction of a Ge core in the Si-QD, electrons are stably retained in the Si clad and holes in the Ge core. The ionized impurity doping is effective in managing the bias conditions for stably charged states. Discrete charged states in the Si-QDs floating gate are confirmed from multiple-step charging and discharging characteristics of MOS capacitors and FETs.

Acknowledgments

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