

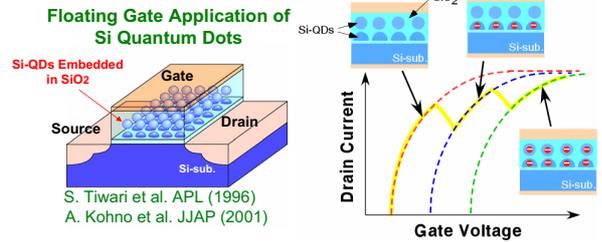
Characterization Electronic Charged States of Si-based Quantum Dots for Multi-valued MOS Memories

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Hiroshima University

- Motivation & Background
- Electron Injection to & Extraction from Single Si-QD with & without a Ge core
 - ➔ Surface Potential Change as Evaluated by an AFM Kelvin Probe Technique
- Floating Gate Application
 - ➔ C-V & I-V Characteristics of MOS Capacitors
 - ➔ Id-Vg & Id-t Characteristics n-MOSFETs
- Summary

Collaborators : K. Makihara, M. Ikeda, Y. Darma, T. Shibaguchi, K. Takeuchi, Y. Shimizu, R. Nishihara

Si-QDs Floating-Gate MOS Memories — Multivalued & Low-Voltage Operations at Room Temp. —



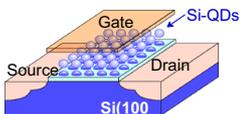
★ Control of Discrete Charged States in Si-QDs

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Electrical Interaction & Coupling among Electronic States in Neighboring QDs

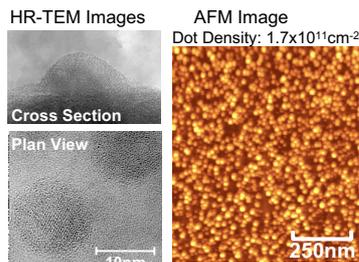
Key Issues on Si-QDs Formation for Floating Gate Application

- The areal dot density comparable to the electron concentration in channel (higher than $\sim 10^{11} \text{cm}^{-2}$)

★ Uniformity in Size & Spatial Distribution

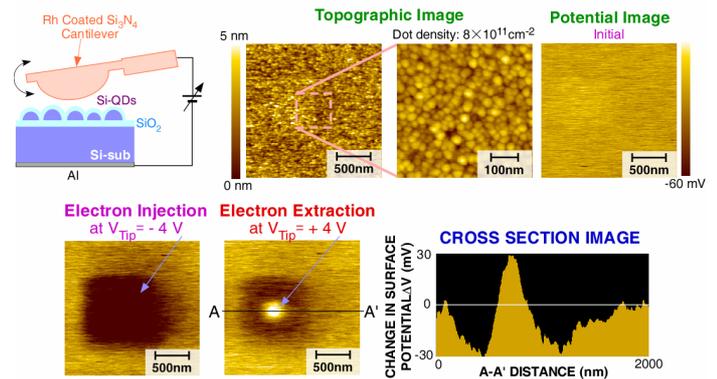


Spontaneous Formation of nc-Si on SiO2 by LPCVD



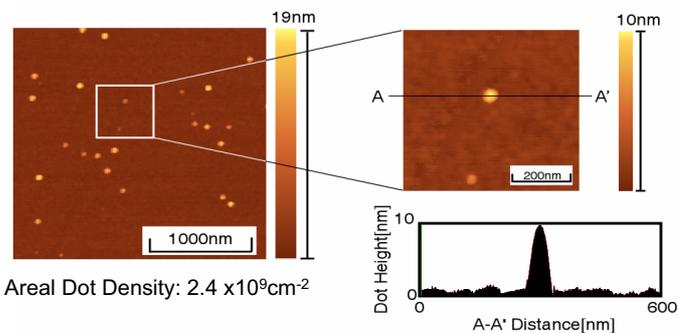
on as-grown SiO2 600°C, 0.2Torr, 36s
on HF-treated SiO2 560°C, 0.2Torr, 90s
S.Miyazaki et al. TSF (2000)

Surface Potential Changes due to Electron Charging & Discharging of Si Dots on 3nm-thick SiO2/p-Si(100) as Evaluated by an AFM/Kelvin Probe Technique

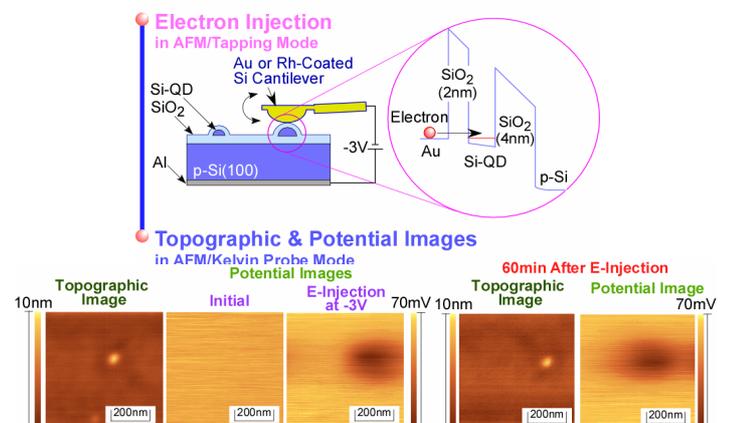


AFM Images of an Isolated Si Quantum Dot

in AFM/Tapping Mode

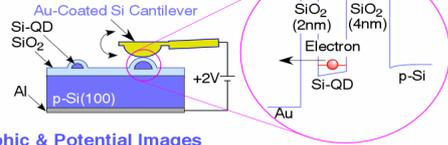


Electron Injection to Single Si-QD



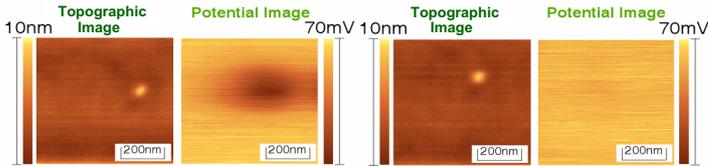
Electron Emission from Charged Single Si-QD

Electron Emission
In AFM/Tapping Mode



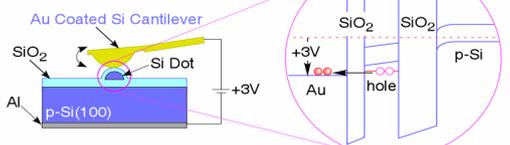
Topographic & Potential Images
In AFM/Kelvin Probe Mode

60min After E-Injection in CR Air at RT

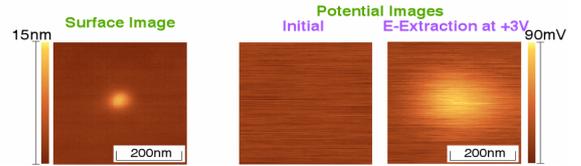


Electron Extraction from Neutral Single Si-QD

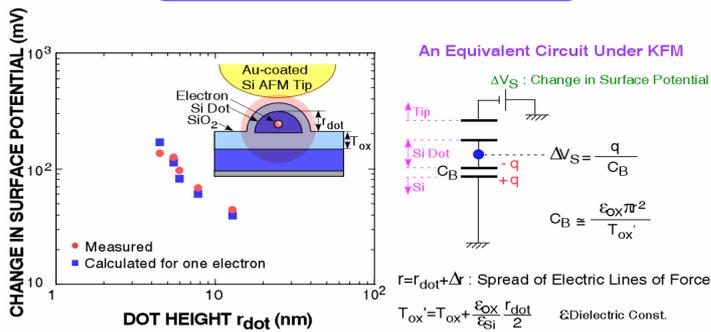
Electron Extraction
In AFM/Tapping Mode



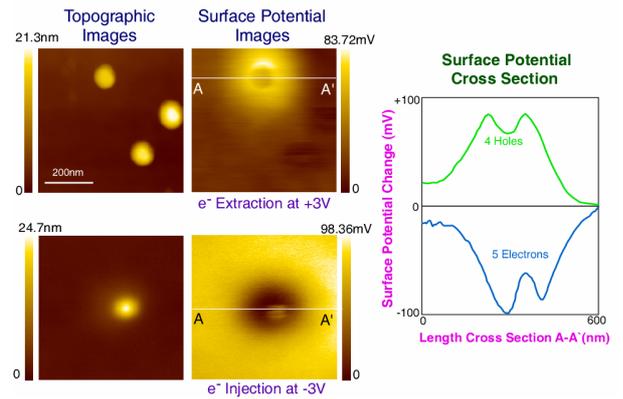
Topographic & Potential Images
In AFM/Kelvin Probe Mode



Dot Size Dependence of Surface Potential Changed by Electron Injection

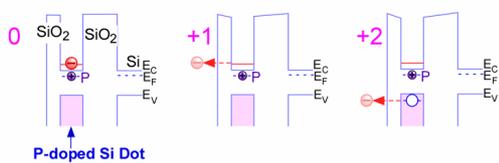


Electron Injection and Extraction from Neutral Pure-Si Dot



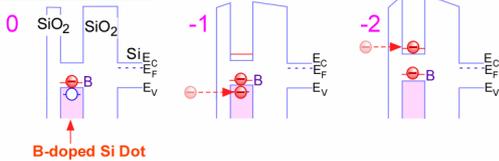
Impact of Impurity Doping into Si-QDs on their Charged States

★ P-doped Si dots



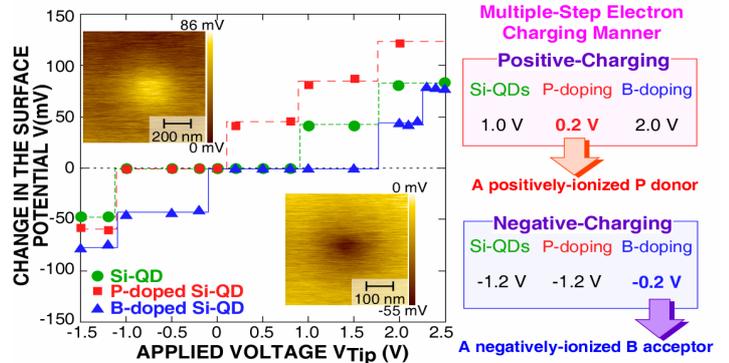
P-doped Si Dot

★ B-doped Si dots

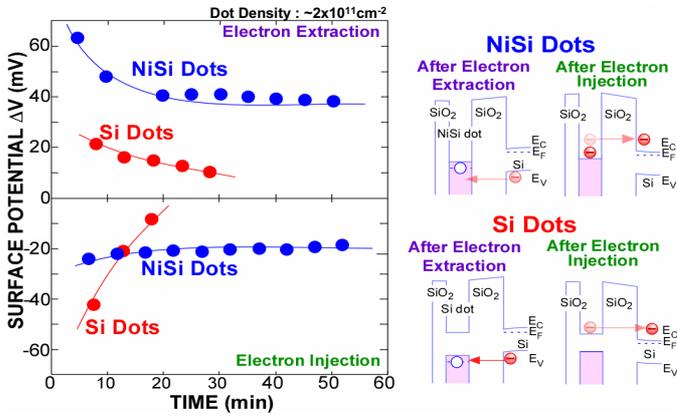


B-doped Si Dot

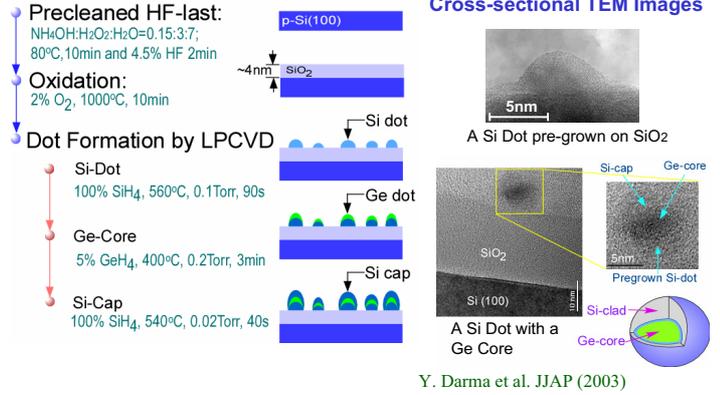
Surface Potential Change for Undoped, P-doped & B-doped Si Quantum Dots / SiO2(4nm) / n+-Si(100) as a Function of Tip Bias



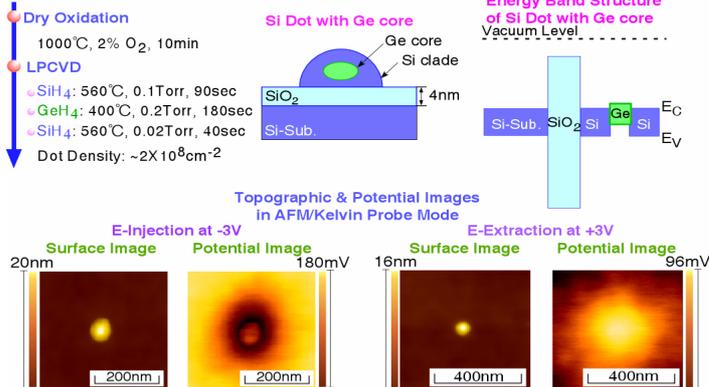
Comparison between Charge Retention Characteristics of pure Si-QDs and NiSi QDs



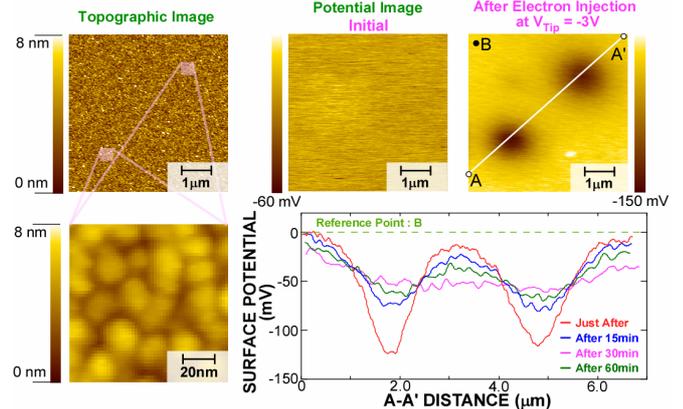
Formation of Si Dots with a Ge Core



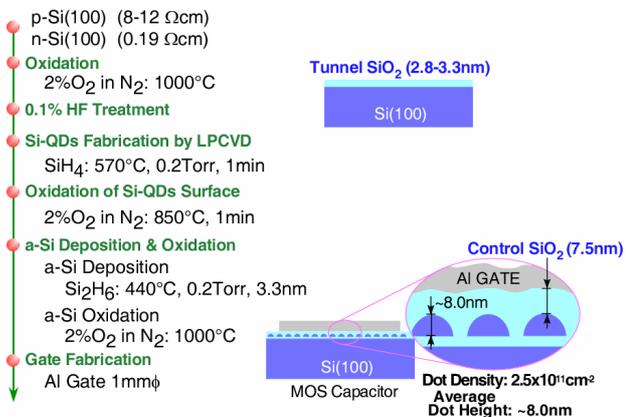
Characterization of Electron Charging into an Isolated Si Dot with Ge core



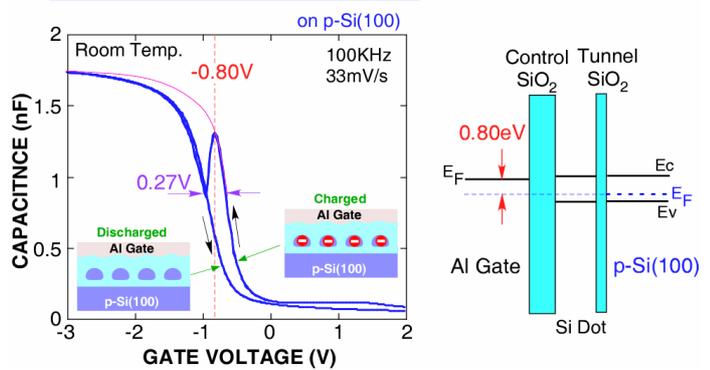
Discharging & Spreading of Electrons Injected into 3-Stacked Si-QDs/ SiO_2 Formed on 4nm-thick SiO_2 /p-Si(100)



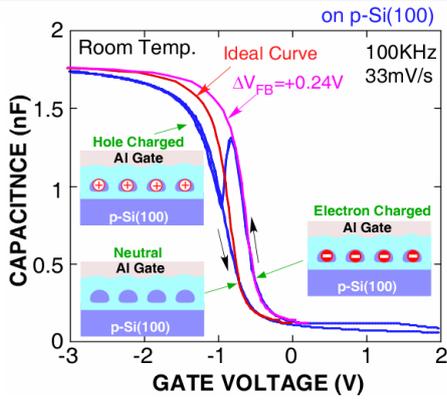
Fabrication of Si-QDs Floating Gate MOS Capacitors



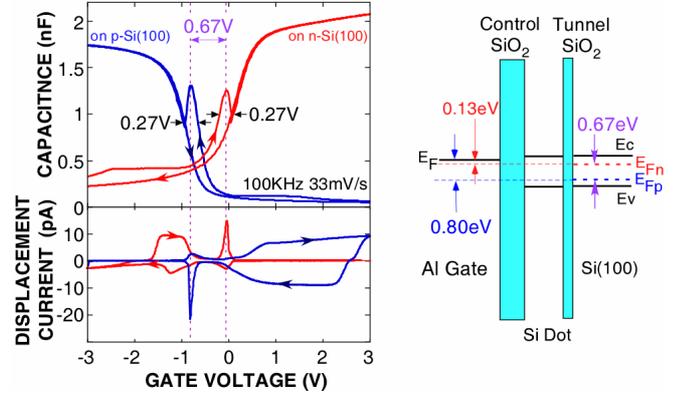
C-V Characteristics of a MOS Capacitor with Si-QDs Floating Gate



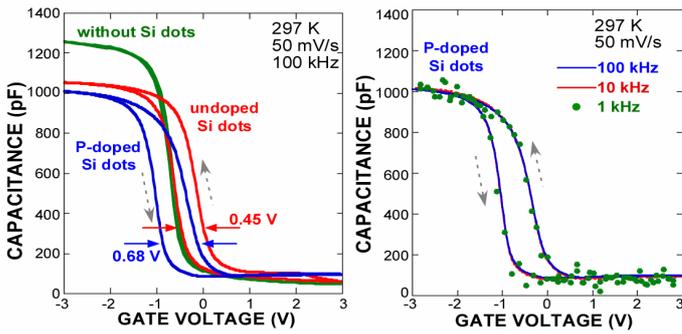
Comparison between Measured and Simulated C-V Curves for Si-QDs Floating Gate MOS Capacitor



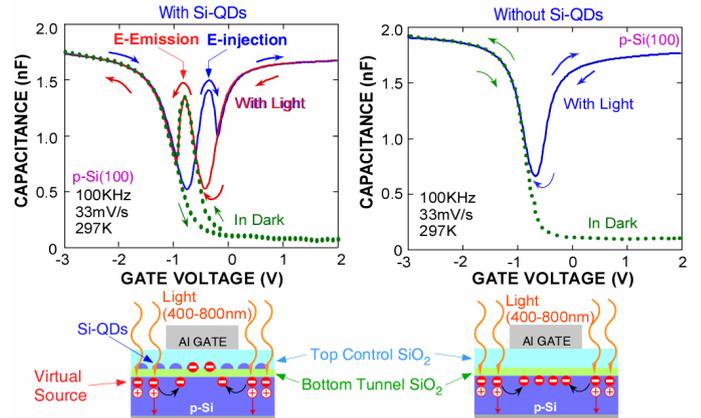
C-V & I-V Characteristics of Si-QDs Floating Gate MOS Capacitors Fabricated on p-Si(100) & n-Si(100)



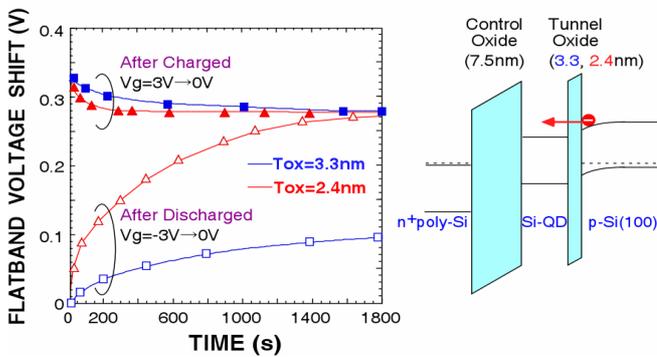
Capacitance-Voltage Characteristics of Undoped & P-doped Si-QDs Floating Gate MOS Capacitors



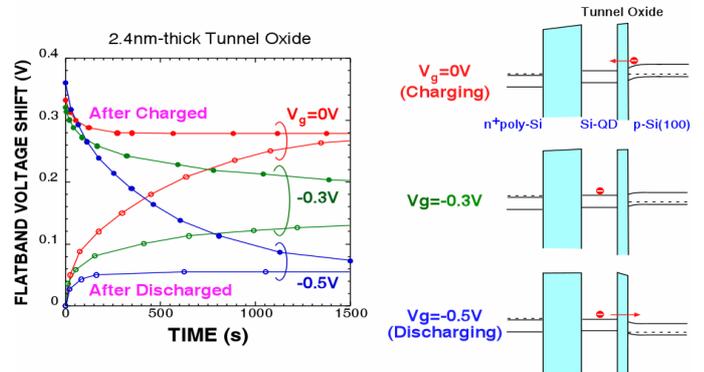
C-V Characteristics of MOS Capacitors with & w/o Si-QDs Floating Gate Measured in Dark and under Cold Light Irradiation



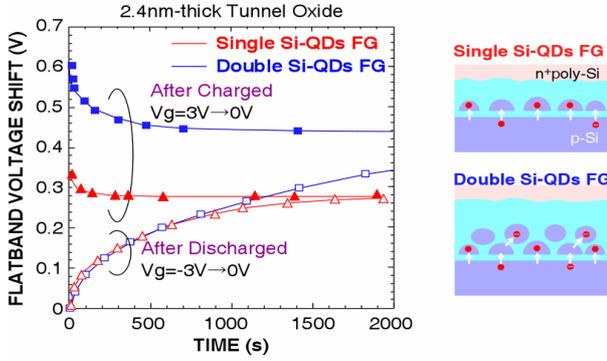
Retention Characteristics on ΔV_{FB} for Single Si-QDs Floating Gate



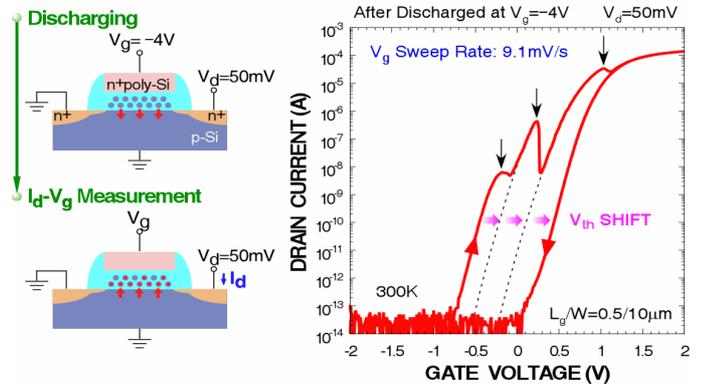
Gate Voltage Dependence of Retention Characteristics



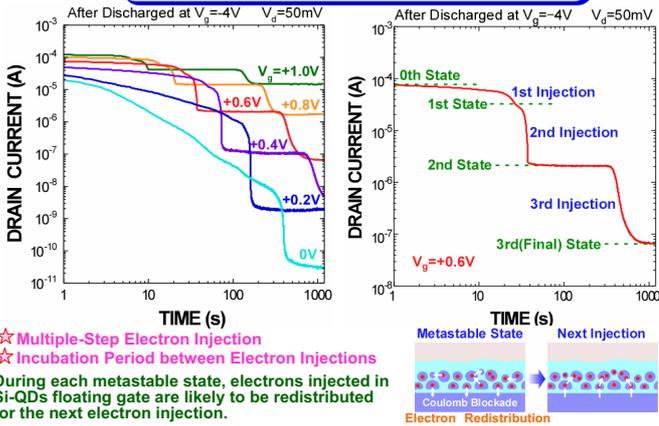
Retention Characteristics on ΔV_{FB} for Single or Double Si-QDs Floating Gate



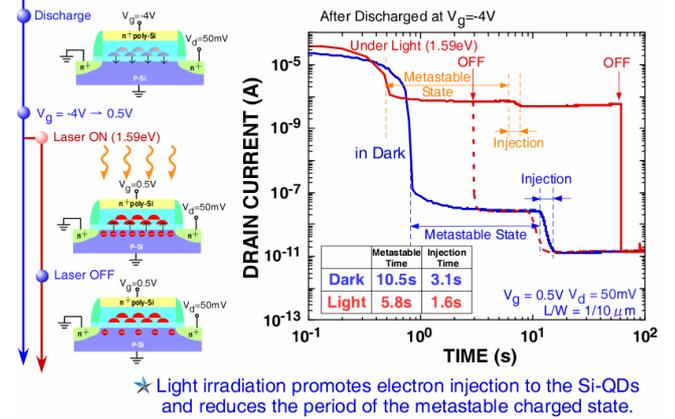
I_d - V_g Characteristics for MOSFET with Doubly-Stacked Si-QDs Floating Gate



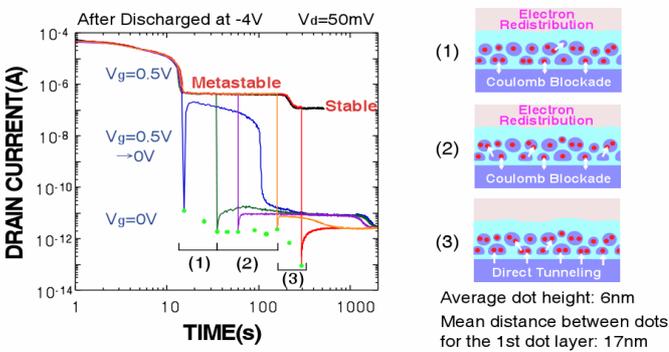
Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate



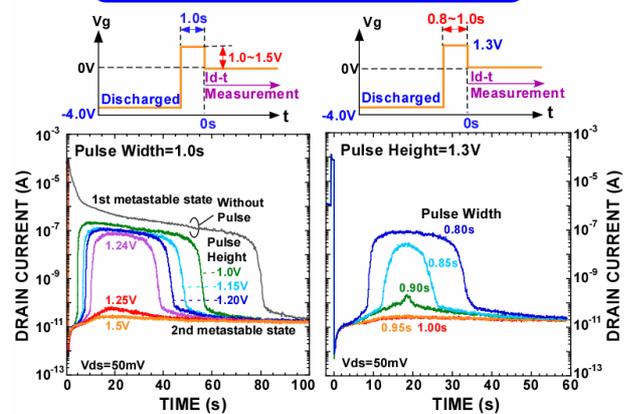
I_d -t Characteristics in Dark and under Light Irradiation



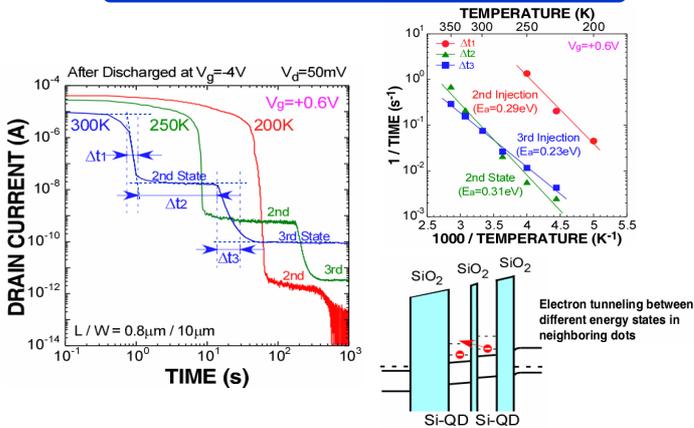
Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate



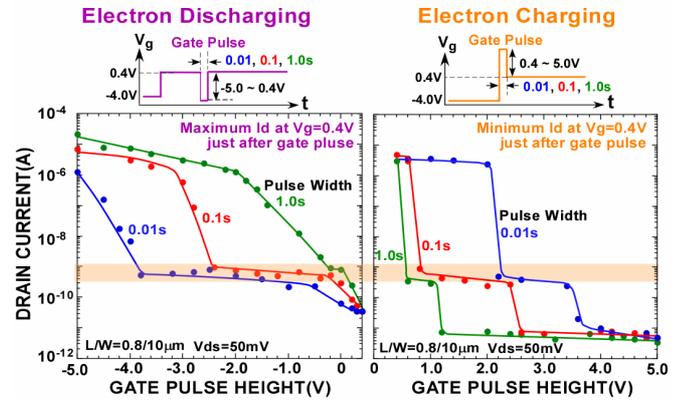
I_d -t Characteristics after Applying Pulsed Gate Biases at Different Pulse Heights & Widths



Temperature Dependence of I_d -t Characteristics



Changes in Drain Current by Applying Pulsed Gate Bias for Charging & Discharging



SUMMARY

Electron Injection to & Extraction from Isolated Si-based QD

- **Si-QD: Single Electron Storage at RT**
Verification of Coulomb Repulsion among Charges Stored in single Si-QD
Control of Charged States with Ionized Impurities
 - **Si-QD with a Ge Core :**
Storage of Electrons in the Si Clad & Holes in the Ge Core
- MOS Cap. and n-MOSFETs with Si-QDs Floating Gate
- Room Temperature Memory Operation
 - ★ Multistep Electron Charging & Discharging

Well-defined & Multivalued Memory Operation

- ➔ Optimization of Dot Size & Oxide Thickness
- Control of Dot Arrangement

Acknowledgements

This work was supported in part in Grant-in Aids for Scientific Research of Priority area (A) and for the 21st Century COE program "Nanoelectronics for Tera-bit Information Processing" from the Ministry of Education, Culture, Sports, Science and Technology.