Characterization Electronic Charged States of Si-based Quantum Dots for Multi-valued MOS Memories

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Motivation & Background
- Electron Injection to & Extraction from Single Si-QD with & without a Ge core
  - Surface Potential Change as Evaluated by an AFM Kelvin Probe Technique

Floating Gate Application
- C-V & I-V Characteristics of MOS Capacitors
- Id-Vg & Id-t Characteristics n-MOSFETs

Summary


Si-QDs Floating-Gate MOS Memories
- Multivalued & Low-Voltage Operations at Room Temp.

Control of Discrete Charged States in Si-QDs
- Electrical Interaction & Coupling among Electronic States in Neighboring QDs

Key Issues on Si-QDs Formation for Floating Gate Application

- The areal dot density comparable to the electron concentration in channel (higher than \(10^{11}\text{cm}^{-2}\))
- Uniformity in Size & Spatial Distribution

Spontaneous Formation of nc-Si on SiO\(_2\) by LPCVD

- HR-TEM Images
- AFM Image
- Cross Section
- Plan View
- on as-grown SiO\(_2\)
  - 600° C, 0.2 Torr, 36s
- on HF-treated SiO\(_2\)
  - 560° C, 0.2 Torr, 90s

S. Miyazaki et al. TSF (2000)

AFM Images of an Isolated Si Quantum Dot in AFM/Tapping Mode

Areal Dot Density: 2.4 x \(10^{9}\text{cm}^{-2}\)

Electron Injection to Single Si-QD

- Topographic & Potential Images
- 60min After E-Injection

Electron Injection in AFM/Tapping Mode

Aul or Rh-Coated Si Cantilever

-electron injection

Si-QD (2nm)

SiO\(_2\) (4nm)

p-Si

Topographic Image

Initial

E-injection at 3V

70mV

10m

Topographic Image

Potential Image

10nm

200nm

200nm

200nm
Comparison between Charge Retention Characteristics of pure Si-QDs and NISi QDs

Dot Density: ~2x10^11 cm^-2

Electron Extraction

Surf ace Potential (V)

Comparison of NiSi Dots and Si Dots after Electron Injection

NiSi Dots

Si Dots

Cross-sectional TEM Images


Characterization of Electron Charging into an Isolated Si Dot with Ge Core

Dry Oxidation
1000°C, 2% O2, 10min

LPCVD
SiH4: 500°C, 0.1 Torr, 60sec
GeH4: 400°C, 0.2 Torr, 18sec
SiH4: 560°C, 0.02 Torr, 40sec

Dot Density: ~2x10^12 cm^-2

Energy Band Structure of Si Dot with Ge Core

Formation of Si Dots with a Ge Core

Pre-cleaned HF-last:
NH3OH+H2O+O2:0:15:3:7;
80°C, 10min and 45% HF 2min

Oxidation:
2% O2, 1000°C, 10min

Dot Formation by LPCVD
Si-Dot
100% SiH4, 560°C, 0.1 Torr, 50s
Ge-Core
5% GeH4, 400°C, 0.2 Torr, 3min
Si-Cap
100% SiH4, 540°C, 0.02 Torr, 40s

Discharging & Spreading of Electrons Injected into 3-Stacked Si-QDs/SiO2 Formed on 4nm-thick SiO2/p-Si(100)

Topographic Image
Potential Image

After Electron Injection at Vgs = 3V

Surface Potential (mV)
150 mV

Fabrication of Si-QDs Floating Gate MOS Capacitors

p-Si(100) (8-12 Ωcm)
-n-Si(100) (0.19 Ωcm)

Oxidation
2% O2 in N2: 1000°C
0.1% HF Treatment

Si-QDs Fabrication by LPCVD
SiH4: 570°C, 0.2 Torr, 1min

Oxidation of Si-QDs Surface
2% O2 in N2: 850°C, 1min

a-Si Deposition & Oxidation
a-Si Deposition
SiH4: 440°C, 0.2 Torr, 3.3nm
a-Si Oxidation
2% O2 in N2: 1000°C

Gate Fabrication
Al Gate 1nm

C-V Characteristics of a MOS Capacitor with Si-QDs Floating Gate

Room Temp.
100KHz
33mV/s

Capacitance (fF)

p-Si(100)
0.80V
0.27V

Control Tunnel SiO2
Si Gate
Al Gate
p-Si(100)

Dot Density: 2x10^10 cm^-2
Dot Height: ~8.0nm

MOS Capacitor
During each metastable state, electrons injected into Si-QDs floating gate are likely to be redistributed for the next electron injection.

Electron Redistribution Incubation Period between Electron Injections

Multiple-Step Electron Injection

During each metastable state, electrons injected into Si-QDs floating gate are likely to be redistributed for the next electron injection.

Light irradiation promotes electron injection into the Si-QDs and reduces the period of the metastable charged state.

Transient $I_d$ Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate

Average dot height: 6nm
Mean distance between dots for the 1st dot layer: 1.7nm
**SUMMARY**

- Electron Injection to & Extraction from Isolated Si-based QD
  - Si-QD: Single Electron Storage at RT
  - Verification of Coulomb Repulsion among Charges Stored in single Si-QD
  - Control of Charged States with Ionized Impurities
- Si-QD with a Ge Core:
  - Storage of Electrons in the Si Clad & Holes in the Ge Core
  - MOS Cap. and n-MOSFETs with Si-QDs Floating Gate
- Room Temperature Memory Operation
- Multistep Electron Charging & Discharging

Well-defined & Multivalued Memory Operation
- Optimization of Dot Size & Oxide Thickness
- Control of Dot Arrangement

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