Formation Techniques for Three-Dimensional MOS Beam-Channel Transistor

Hideo Sunami and Kiyoshi Okuyama
Research Center for Nanodevices and Systems, Hiroshima University
1-4-2 Higashi-Hiroshima, Hiroshima 739-8527, Japan
E-mail: sunami@sxsys.hiroshima-u.ac.jp

Abstract

Development of three-dimensional (3-D) MOS transistors are summarized focusing on processing techniques to realize tall silicon beam with very high aspect-ratio, overlaying gate formation, and 3-D plasma doping into the tall beam.

1. Introduction

3-D transistors recently proposed[1-3] have focused on their miniaturization in response to the requirement for further scaling of planar MOS transistor. While, the transistor of 5 nm in gate length has been developed[4] even though its performance does not deserve its miniature size.

Besides the transistor scaling, there exists another application of 3-D transistor for power transistor integrated in LSI. Since the power transistor consumes a lot of planar area responding to power requirement particularly in area-conscious LSI, more power in less planar area must be desirable.

Thus, some possible application of 3-D MOS transistor named beam-channel transistor, BCT[5-7] is proposed in this study. Its bird's eye view is shown in Fig. 1. This BCT has 1-μm-high beam, drive current can be expected to be 20-times higher than that of FINFET[3] of which beam height is 50 nm. Subjects for realization of BCT are listed in Table 1.

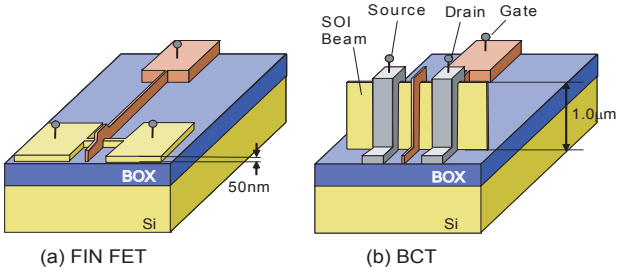

Fig. 1 FINFET (a) as a representative of 3-D transistor and a beam channel transistor, BCT studied.

Difficulty in fabricating tall 3-D transistor rather depends on aspect ratio of the beam than absolute height of the beam. In this sense, a figure of merit of beam height / gate length, $f_{H/L}$ is shown in Fig. 2 regarding transistors realized in this study. One target at present is $f_{H/L}$ of 10 when beam height, H_B is 500 nm and gate length, L_g is 50 nm.

Table 1 Development items for 3-D MOS transistor with relatively tall beam.

Subject A: delineation of tall Si beam
Subject B: gate formation around tall Si beam
Subject C: impurity doping to tall Si beam
Subject D: source/drain contact to tall Si beam

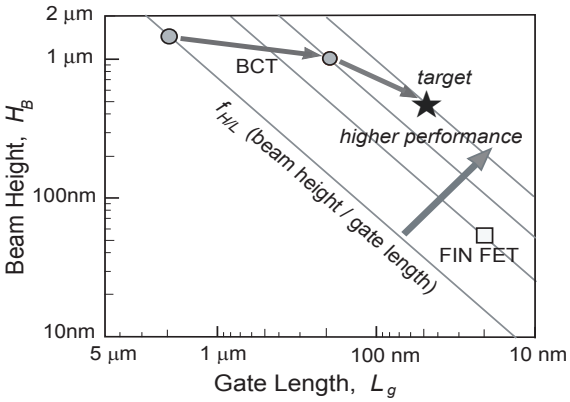

Fig. 2 A proposed figure of merit of beam height / gate length, $f_{H/L}$ closely related to difficulty in fabricating 3-D transistor.

2 Experimental

2.1 Subject A: delineation of tall Si beam

It is possible to obtain high aspect-ratio Si beam with state-of-the-art present directional reactive ion etching, RIE. However, anisotropic etching with tetramethylammoniumhydroxide, TMAH must be adequate to realize much taller and steeper beam only in a case that (110) surface can be used for substrate. Due to its very low etch rate for (111), as shown in Tabe 2, almost perfect perpendicular sidewall can be obtained on (110) Si substrate.

Table 2 Etch rates of TMAH (2.5% aqueous solution at 75°C).

Material	Etch Rate (nm/min)	Ratio
(110) Si	606	30
(111) Si	30	1
SiO_2	0.8	0.04

Using this etchant, a corrugated channel transistor, CCT with multiple Si beams has been succcessfully fabricated[5,6] on (110) substrate as shown in Fig. 3. The height and the width of the beam are 900 nm and 82 nm, respectively. Obtained drain currents of CCT's are shown in Fig. 4.

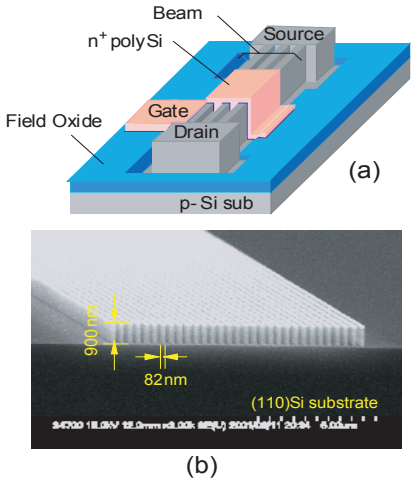

Fig. 3 A bird's eye view of corrugated channel transistor, CCT (a) and an SEM image of etched 31 Si beams formed on (110) substrate with TMAH etchant.

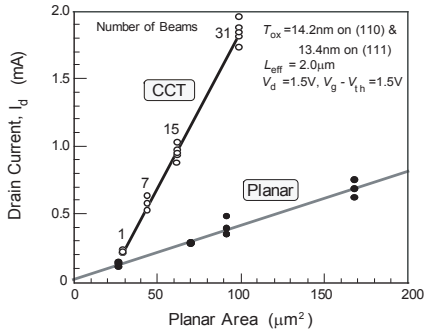

Fig. 4 Obtained drain currents of CCT's with number of beams of from 1 to 31. Almost 5-fold increase is realized compared to planar transistor at a planar area of 100 μm^2.

2.2 Subject B: delineation of gate electrode overlaying tall Si beam

The use of conventional anisotropic dry etching to delineate polysilicon gate overlaying Si beam gives rise to residues on sidewalls of the beam as shown in Fig. 5(a). Thus, isotropic etching is inevitable at present, as shown in Fig. 5 (b).

To overcome the problem, a novel technique has been developed[7]. This technique, named SELOCS[8], makes it possible to wrap the polysilicon gate with its own oxide utilizing impurity enhanced oxidation, IEO[9]. The enhancement occurs with highly doped Si at low-temperature wet oxidation. In certain condition more than 10-fold enhancement is possible.

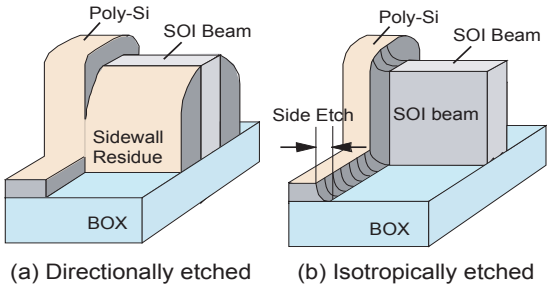

Fig. 5 Gate electrodes formed by anisotropic etching (a) or isotropic etching (b). Cross-sectional TEM images for oxide thinning at beam edges.

A cross section and I_d-V_g characteristics are shown in Figs. 6 and 7, respectively for beam channel SOI transistors.

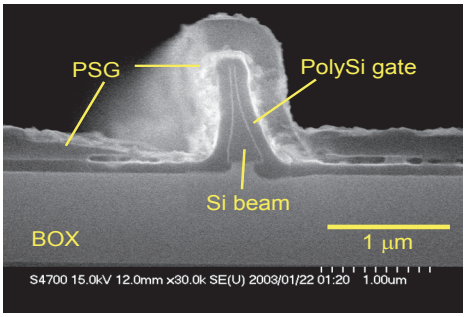

Fig. 6 A cross section of SOI beam channel transitor.

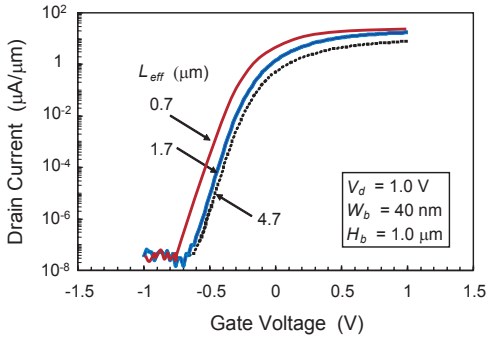

Fig. 7 I_d-V_g characteristics of BCT with 1.0-μm high and 40-nm thick SOI beam and 0.7-μm channel length. No channel implantation causes weak cut-off.

2.3 Subject C: impurity doping to high Si beam

Even though utilizing oblique implantation, there exists certain limitation to conventional ion implantation technique, I/I to make uniform doping to high and dense Si beams. To cope with the problem, nearly isotropic plasma doping, PD is applied in this study.

A comparison of impurity profiles of I/I and PD is shown in Fig. 9 at the same applied voltage of 700 V.

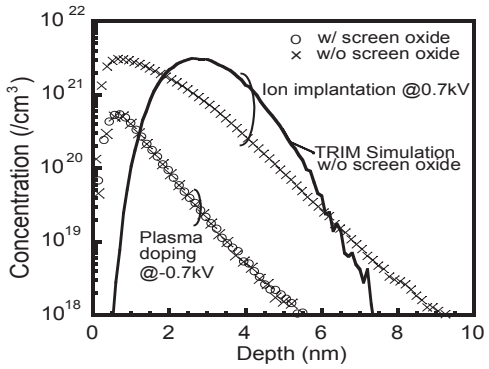

Fig. 8 Arsenc SIMS profiles for ion implantation and plasma doping at the same applied voltage of 700 V.

A Beam-Channel Transistor, BCT is fabricated with this arsenic-plasma doping (PD) into source/drain region in comparison with $POCl_3$ gaseous doping (GD). A cross section of a typical BCT obtained is shown in Fig. 9. Note that the upper edges of the BCT are rounded. It is clarified in this work that plasma atom bombardment make the edge rounding causing device performance degradation .

A crude classification of device failures is summarized in Fig. 10. It is characterized that the gate leakage only ocurred in BCT. Thicknesses of BCT and planar gate oxides simultaneously formed are 9 nm and 13 nm, respectively, because the BCT gate oxide is formed on (111) face and that of planar, (110).

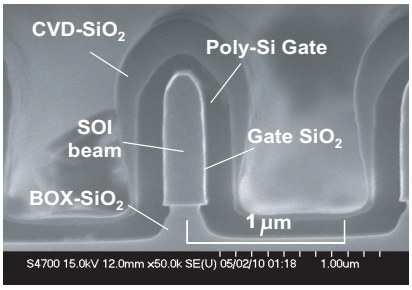

Fig. 9 Obtained beam-channel transistor structure with plasma doping. Rounded top edges are estimated to be caused by Ar ion bombardment.

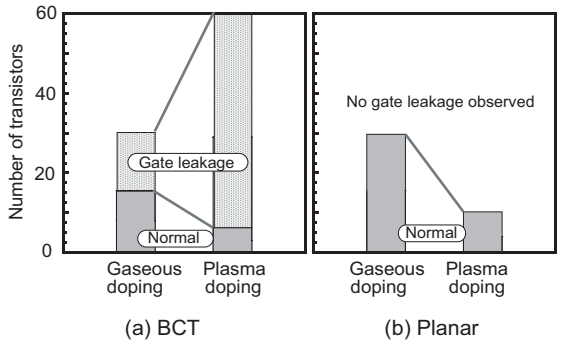

Fig. 10 A crude classification of device failures.

Typical I_d-V_g characteristics are shown in Fig. 11 . In GD case, normal performance is obtained, however, PD gives birth to anomalously low performance. As previously discussed, it was already recognized that the Ar plasma doping used in this study caused silicon sputtering resulting in rounded top edges of SOI beam[9]. The influence of the sputtering energy is also recognized on device performance in terms of gate leakage and transconductance degradation.

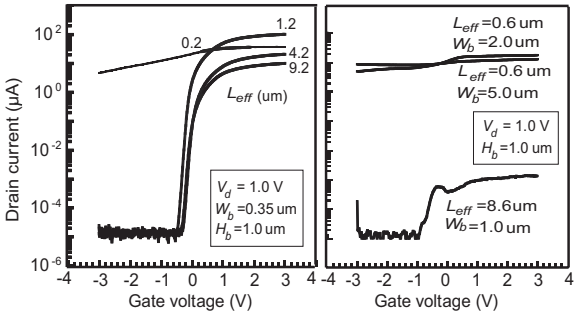

Fig. 11 Typical I_d-V_g characteristics of BCT with gaseous or plasma dopings.

2.4 Subject D: source/drain contact to high Si beam

When a contact to source and drain (S/D) is formed only on the top surface of the beam, a part of source current flowing at the bottom portion suffers from parasitic resistance of the source. This causes perfor-mance degradation of the transistor. To overcome the problem, appropriate methods efficient to reduce the resistance should be employed. These are as follows:

(1) silicidation of S/D,
(2) elevated S/D with Si and/or Ge, and
(3) metal wrapping around S/D.

Preliminary experiment for silicidation has been carried out in this study. Phosphorus-doped Si beam is silicided with 100-nm thick sputtered Ni after vacuum baking at 500^{O}C for 30 min, as shown in Fig. 12.

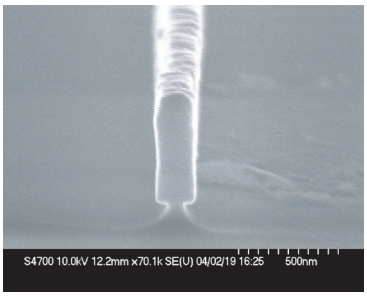

Fig. 12 Ni-silicided Si beam of which height/width is 550nm/180nm.

Estimated resistivity of phoshprus-doped Si beam and its silicided layer are:

- n^+-Si beam resistivity = $4.2 \times 10^{-4}\Omega$-cm
- Ni silicide layer resistivity = $2.5 \times 10^{-5}\Omega$-cm

While, it is observed in the experiment that Si atoms in the beam creep into adjacent Ni film through Ni grain boundary resulting in silicide whisker along the boundary, as shown in Fig. 13. It is not yet understood at present what mechanism is dominant for the formation of the whisker and silicide. In practical use of the silicided SOI beam, amount of deposited Ni should be carefully controlled together with removal of adjacent excess Ni film. Otherwise, electrically short circuit may occur among ajacent beams causing fatal failure on LSI's.

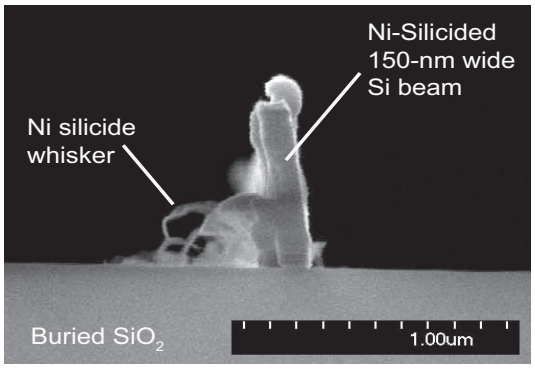

Fig. 13 Residual Ni-silicide whiskers on an SOI beam after removal of unreacted Ni metal witt SPM (H_2SO_4:4+H_2O_2:1).

3 Conclusion

In this study, one set of beam channel transistor, BCT of 1.5-μm beam height and 2.0-μm gate length, and another set of those of 1.0-μm beam height and 0.2-μm gate length are successfully developed. Since BCT with high Si beam can not provide narrow channel width, the BCT is not able to be major component of LSI. Therefore, the BCT is suitable to some applications with big power in small area.

They are:

(1) discrete power transistor,
(2) wireless receiver/transmitter IC integrateing RF power transistor, and
(3) power control transistor for ultra-low power.

Some example concerning item (3) is shown in Fig. 14. This is an idea that a pull-down transistor which is connected in series to a circuit block controls power consumption, stand-by current, and operation speed of the block in time sharing manner.[12] Since it is desirable that on-resistance of the pull-down transistor is as small as possible,

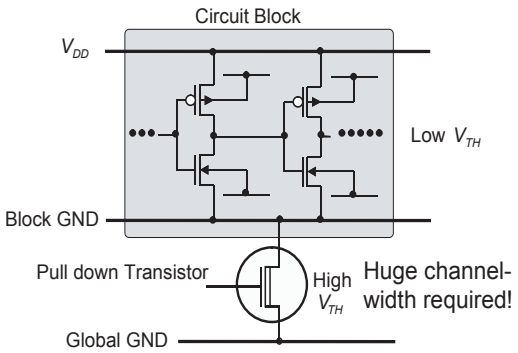

Fig. 14 An idea to control power consumption, stand-by current, and operation speed with each circuit block[9].

BCT which can provide large current in small planar area is suitable with less area penalty.

Based on these fabrication techniques, highly self-alighed triple gate 3-D MOS transistors are successfully developed[13].

Acknowledgement

The authors would like to thank T. Furukawa, A. Katakami, K. Kobayashi, S. Matsumura, A. Sugimura, and K. Yoshikawa for their device fabrication. This work was partly supported by Grant-in-Aids for Scientific Research (B#12555102, A (2) #13025232) from the Ministry of Education, Science, Sports, and Culture, Japanese Government.

Reference

1) D. Hisamoto, T. Kaga, and E.Takeda, IEEE Trans. Electron Devices, 38, pp. 1419-1425, 1991.
2) H-S. P. Wong, D. Frank, and P. Solomon, IEDM Tech. Dig, pp. 407-410, 1998.
3) Y-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T-J King, J. Bokor, and C. Hu, IEDM Tech. Dig. pp. 421-424, 2001.
4) H. Wakabayashi, S. Yamagami, N. Ikezawa, A. Ogura, M. Norihiro, K. Artai, Y. Ochiai, K. Takeuchi, T. Yamamoto, and T. Mogami, IEDM Tech. Dig., pp. 989-992, 2003.
5) T. Furukawa, H. Yamashita, and H. Sunami, Jpn. J. Appl. Phys., Vol. 42, pp. 2067-2072, 2003.
6) H. Sunami, T. Furukawa, and T. Masuda, Sensors and Actuators A111, pp. 310-316, 2004.
7) A. Katakami, K. Kobayashi, and H. Sunami, Jpn. J. Appl. Phys., Vol. 43, pp. 2145-2150, 2004.
8) H. Sunami and M. Koyanagi, Supplement to Japan. J. Appl. Phys., Vol. 18-1, pp. 255-260, 1979.
9) H. Sunami, J. Electrochem. Soc., Vol. 125, pp. 892-897, 1978.
10) K. Kobayashi, T. Eto, K. Okuyama, K. Shibahara, and H. Sunami, Jpn. J. Appl. Phys. Vol.44 2273-2276, 2005.
11) S. Matsumura, A. Sugimura, K. Okuyama, and H. Sunami, to be published in Proc. ADMETA, 2006.
12) T. Inukai, M. Takamiya, K. Nose, H. Kawaguchi, T. Hiramoto, T. Sakurai, CICC Tech. Dig., pp. 409-412, 2000.
13) K. Okuyama, Yoshikawa, and H. Sunami, Ext. abs. SSDM Ext. Abs. pp.506-507, 2006.