# Formation Techniques for Three-Dimensional MOS Beam-Channel Transistor

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**Introduction**
**Subject A: Delineation of tall Si beam**
**Subject B: Delineation of gate electrode overlaying tall Si beam**
**Subject C: Impurity doping to tall Si beam**
**Subject D: Source/drain contact to tall Si beam**
**Summary**

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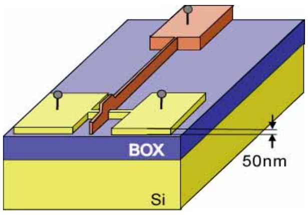
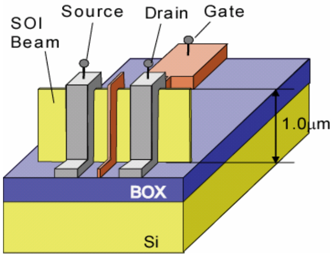
## Beam-Channel Transistor



**FINFET**



**BCT (beam-channel transistor)**

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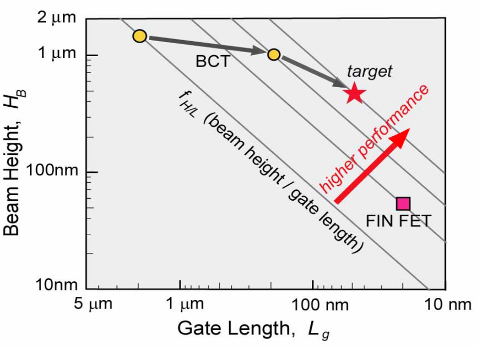
## Figure of merit for 3-D transistor structure

**Beam Height / Gate Length = $H_B/L_g$**



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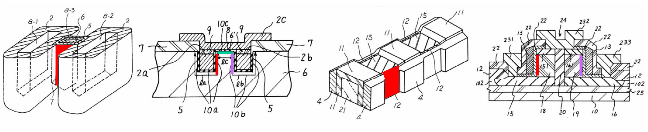
## Some 3-D transistor ideas in good old days

**Patents applied by the author**



(a) Sidewall channel MOS transistor
Applied in 1975
JP#1344386

(b) Tri-gate MOS transistor
Applied in 1983
disclaimed

(c) Beam sidewall Channel MOS transistor
Applied in 1983
USP#4937641

(d) Vertical channel CMOS transistor
Applied in 1983
USP#4670768

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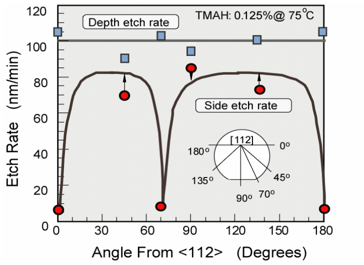
## Anisotropic etching solution

**TMAH (tetra methyl ammonium hydroxide) for (110) surface**



Etch rates of TMAH
(2.5% aqueous solution at 75°C).

| Material | Etch Rate | Ratio |
|---|---|---|
| (110) Si | 606 nm/min | 30 |
| (111) Si | 30 nm/min | 1 |
| $SiO_2$ | 0.8 nm/min | 0.04 |

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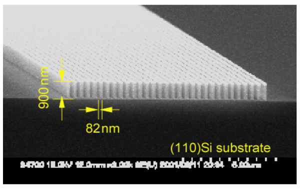
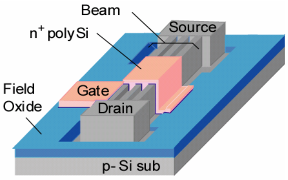
## Corrugated-Channel Transistor, CCT

**A kind of BCT having multiple Si beams**



**31 Si beams on (110) Si substrate etched by TMAH**



**CCT structure**

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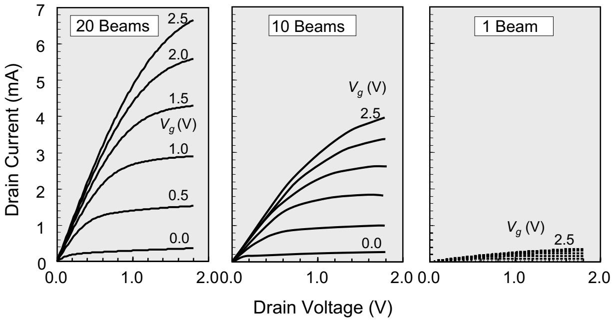
## $I_d$-$V_d$ characteristics of BCT



**10-nm $T_{ox}$, 0.8-µm $L_{eff}$, 40-nm $W_b$, and 1.0-µm $H_b$**

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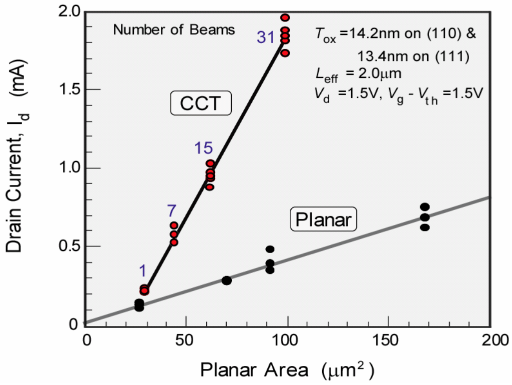
## Quadrupled drivability of CCT



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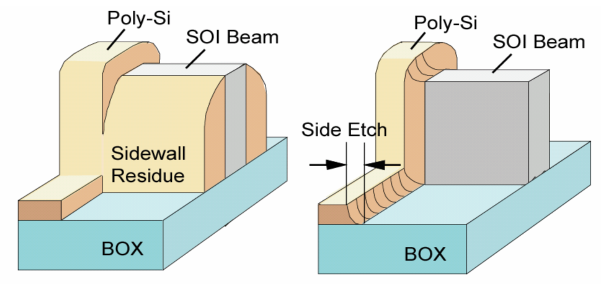
## Sidewall residue caused by directional etching



(a) Directionally etched (b) Isotropically etched

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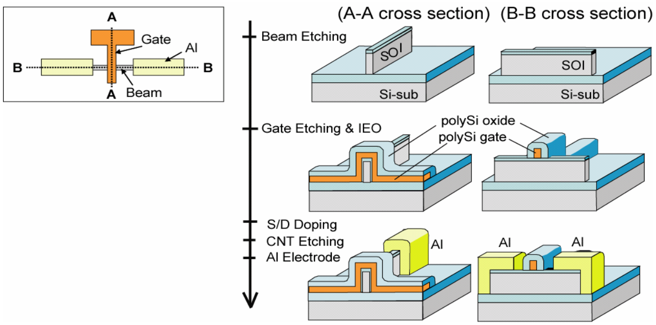
## Selective oxide coating of silicon gate

***Polysilicon gate is covered with its own oxide utilizing impurity-enhanced wet oxidation at lower than 800°C***



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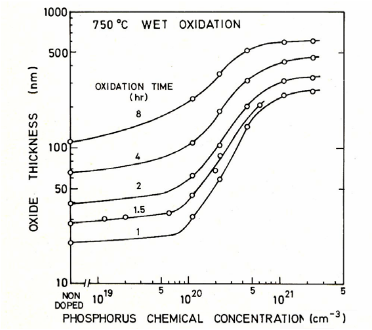
## Impurity-enhanced oxidation, IEO

**Relatively low-temperature wet oxidation rate is strongly enhanced with higher concentration of impurity such as P or As.**



H. Sunami, "Thermal Oxidation of Phosphorus Doped Polycrystalline Silicon in Wet Oxygen," J. Electrochem. Soc., Vol. 125, No. 6, pp. 892-897, 1978.

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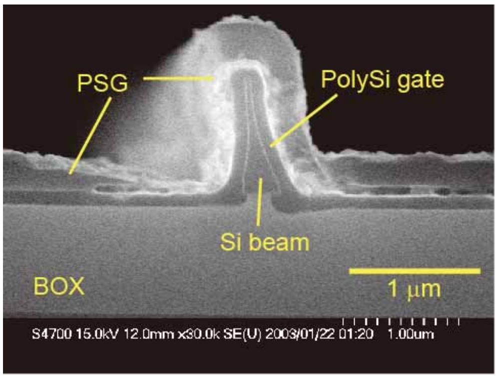
## Beam-channel transistor on SOI



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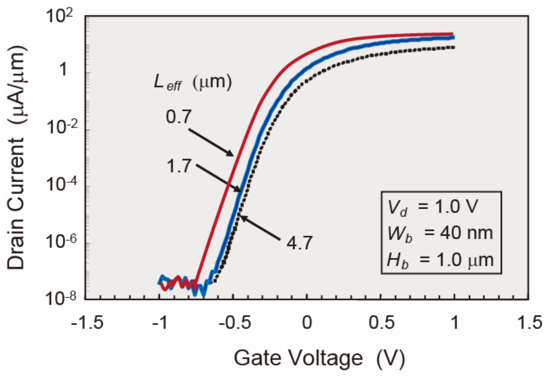
## $I_d$-$V_d$ characteristics of BCT



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## Uniform impurity doping

**Estimated applicability to 3-D doping**

| Doping method | Merits | Demerits |
|---|---|---|
| **Gaseous doping** | **• High dosage**<br>**• Uniform doping** | **• Poor controllability for low-dosage** |
| **Ion implantation** | **• Excellent controllability for dosage** | **• Complexity of oblique and multi-time implantation** |
| **Plasma doping** | **• Fair controllability for low-dosage**<br>**• Uniform doping** | **• Fair controllability for low-dosage** |

***Challenge :*** ***S/D to be formed with $POCl_3$ gaseous doping and extension to be formed with plasma doping***

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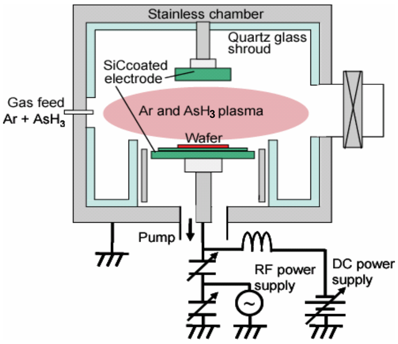
## Plasma doping apparatus used



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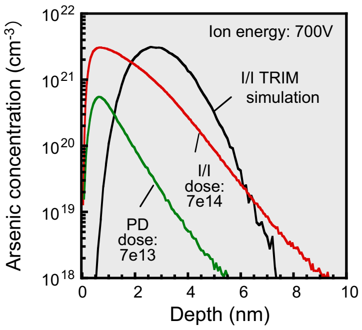
## Arsenic doping profiles

**SIMS profiles of plasma doping and ion implantation**



**Plasma doping: effective dose ~ 1 %**

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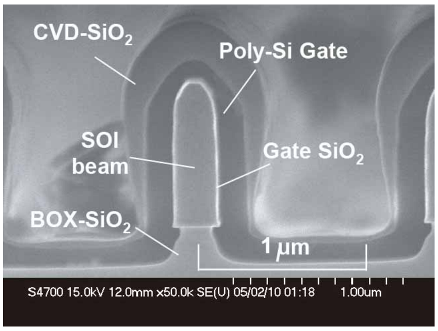
## Completed device cross section



**Note that the top edges are rounded.**

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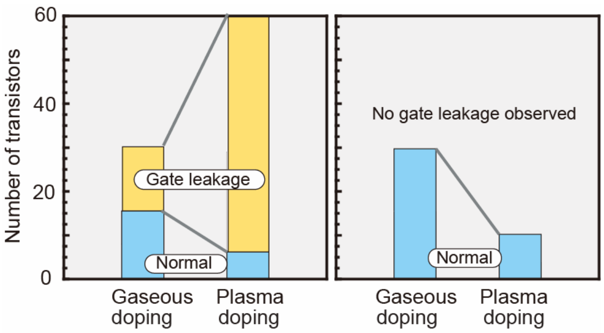
## A crude classification of device failures



(a) BCT (b) Planar

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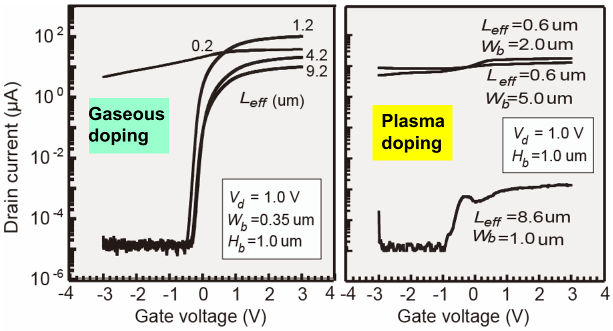
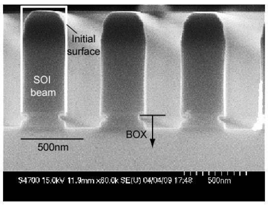
## Degraded device performance

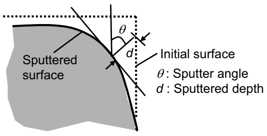


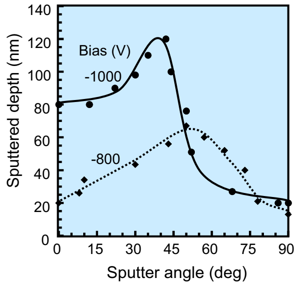
(a) BCT with GD (b) BCT with PD

## An adverse effect of plasma doping : sputtering

Plasma doping bias = -1000V







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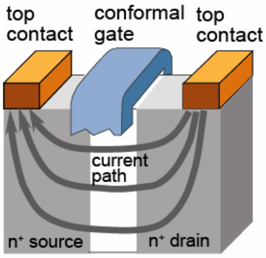
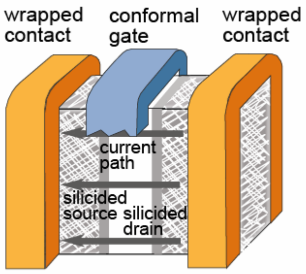
## Importance of wrapped contact



(a) Top contact



(b) Wrapped contact and silicided source/drain

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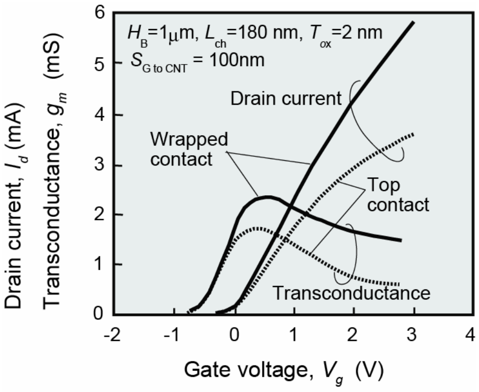
## Advantage of wrapped contact (simulated results)



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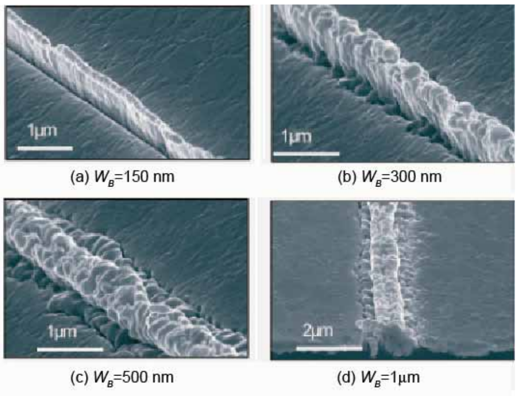
## Deformation of Ni-silicided Si beams



(a) $W_B$=150 nm

(b) $W_B$=300 nm

(c) $W_B$=500 nm

(d) $W_B$=1μm

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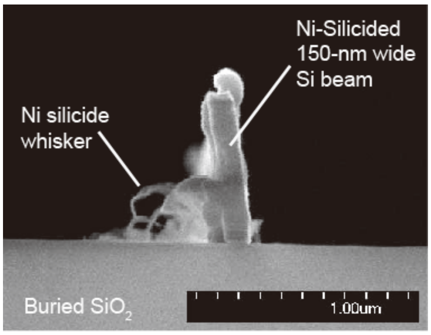
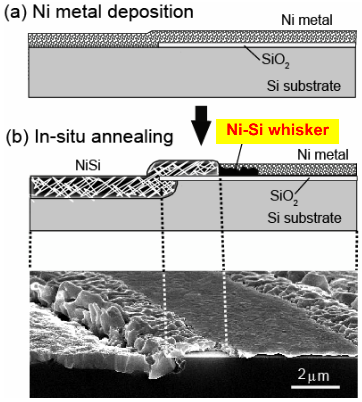
## Application of silicided source/drain

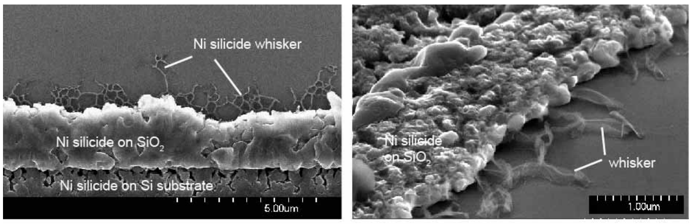


**After unreacted Ni metal film is removed by $H_2O_2$-$H_2SO_4$ mixed solution**

## Verification of Ni-Si whisker formation



## Ni-Si whisker creeping into Ni grain boundaries



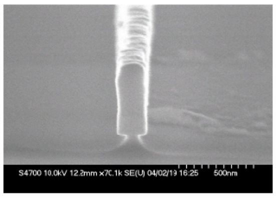
(a) Plan view of front end of Ni-silicide crept up on $SiO_2$ film

(b) Enlarged bird's eye view of Ni-silicide whisker

**After unreacted Ni metal film is removed by $H_2O_2$-$H_2SO_4$ mixed solution**

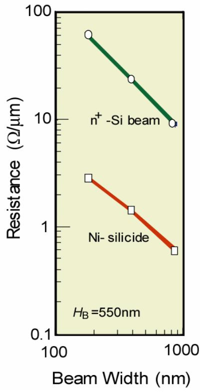
## Application of silicided source/drain

**Ni-silicide formation on Si beam**



Beam height/width＝550 nm/180 nm

| Material | Resistivity (Ω-cm) |
|---|---|
| **$n^+$-Si beam** | **$4.2 \times 10^{-4}$** |
| **Ni silicided beam** | **$2.5 \times 10^{-5}$** |



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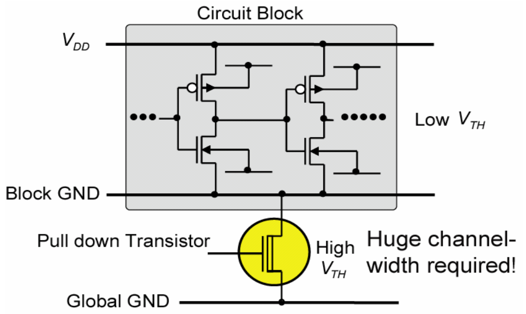
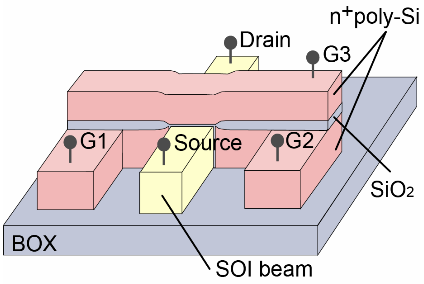
## One of candidates of BCT application

**Power consumption control with simultaneous speed control**

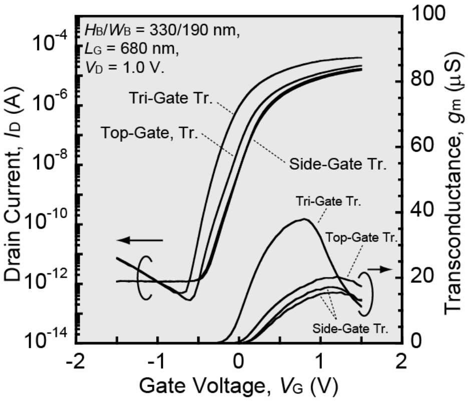


## Challenges to future scaling

**Self-aligned triple gate FIN FET**



## $I_d$-$V_g$ under different gate combination mode



## Summary

Throughout the course of our research, indispensable techniques to realize tall beam-channel transistor have been developed. They are *delineation of silicon beam, delineation of gate electrode, impurity doping, and source/ drain contact, all to tall silicon beam*.

Potential applications are for *discrete power transistor, wireless receiver/transmitter IC integrating RF power transistor, and power-consumption control transistor for ultra-low power LSI's*.

These techniques developed in this study are expected to be applied to future scaling of three-dimensional MOS transistors.

## Acknowlegements

The authors would like to thank T. Furukawa, A. Takase, A. Katakami, K. Kobayashi, S. Matsumura, and K. Yoshikawa for their device fabrication and assistances. They also wish to thank all of colleagues in Research Center for Nanodevices and Department of Semiconductor Integration Science, Hiroshima University.

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