A Single-chip Gaussian Monocycle Pulse Transmitter using 0.18 μm CMOS Technology for Intra/Interchip UWB Communication

Takamaro Kikkawa, Pran Kanai Saha, Nobuo Sasaki and Kentaro Kimoto

Research Center for Nanodevices and Systems, Hiroshima University
1-4-2 Kagamiyama, Higahshi-hiroshima, Hiroshima, JAPAN
Email: kikkawa@sxsys.hiroshima-u.ac.jp

1. Introduction

Scaling for metal interconnects will encounter the limitation in global clock frequency and data transmission rate due to the increases of RC delay of the multilevel metal interconnects. The Cu/low-k technology could solve the existing problems [1], however, it cannot be an ultimate solution for the elimination of the RC delay. A concept of system on a chip will lead to stacked multi-chip packaging and three-dimensional (3D) integrated circuits [2]. To meet the requirements for 3D stacked chip packaging, new interconnection technology must be developed to substitute wire bonding which has large inductance and capacitance. From this point of view, wireless interconnection technologies have been developed [3-9], which can eliminate parasitic RC and enable much higher data rate than metal wire interconnections.

There are several approaches to realize wireless interconnections between chips. Capacitance coupling and inductance coupling can transmit signals between chips with high fidelity in the practical distance less than 300 μm. However, there is an inherent limitation to transmit signals for long distance. On the other hand, electromagnetic wave, which is transmitted and received by use of on-chip integrated antennas, can achieve long distance propagation [3-9]. The target distance in this study for signal transmission between LSI chips is in the order of 1-10 mm. According to Shannon's theorem, the channel data rate (capacity) is proportional to the bandwidth as described in equation (1),

$$C = B \log_2\left(1 + \frac{S}{N}\right) \qquad (1)$$

where C and B are channel capacity and bandwidth, respectively. S/N is signal to noise ratio. Therefore, ultra-wide band (UWB) technology [10] has been developed for high data rate signal transmission between chips. This technology also has advantages of the lower power consumption and the simple circuitry in the case of carrier free impulse radio based UWB (IR-UWB). IR-UWB technology uses ultra-short pulses with low duty cycle in time domain, which has ultra-wide-bandwidth and high center frequency in frequency domain. Generation of ultra-short impulse is a very difficult task and now a major issue towards the development of single chip IR-UWB transceiver system.

The goal of the research is to develop CMOS UWB transmitter and receiver with on-chip integrated antennas for Gaussian monocycle pulse (GMP) transmission.

In this paper, we demonstrate a fully integrated GMP generation circuits in CMOS, and transmission and reception of generated GMP between Si chips by using integrated antennas.

2. GMP Generation and Transmitter Architecture

Figure 1 shows the architecture of IR-UWB transmitter including GMP Generation. The GMP circuit consists of 8 stages differential voltage controlled oscillator (VCO), 8 to 1 multiplexer, triangular pulse generation (TPG) and differentiator. The multiplexer is used here with a view to using the same GMP generation circuit at the receiver side for template synchronization. Schematics of delay cell and differential 2 to 1 multiplexer as building block of VCO and the multiplexer are shown in Figs. 2(a) and 2(b) respectively. In the case of transmitter circuit the multiplexer output select-lines are made all logic high so that the multiplexer selects the output from the last delay cell of the VCO for TPG. The TPG circuit is shown in Fig. 2(c). The triangular pulse (TP) is differentiated to generate GMP. The differentiator is designed using metal-insulator-metal capacitor (MIMCAP) and poly resistor (R) in such a way that it behaves as close as to ideal differentiator. The amplitude of the GMP depends on derivative time constant (RC), rising time (t_r) and falling time (t_f) of TP. The single ended GMP is then converted into differential GMP by using single input dual output (SIDO) amplifier and then amplified by output amplifier as shown in Fig 2(d) for transmission in Si by integrated meander type dipole antenna with the length of 2.98 mm. The SIDO is a differential amplifier which one input is grounded. The source follower is used for impedance matching.

3. Test Chip and Experimental Results

In order to verify GMP generation and transmitter, a test chip is fabricated in TSMC 0.18 μm CMOS technology. The test chip die microphotograph as shown in Fig. 3 is bonded on printed circuit board for wiring of dc bias voltage. GMP measurement is carried out using Cascade fine pitch microprobe (FPM-100x). The measured GMP before SIDO circuit is shown in Fig. 4, which shows that GMP of 123 mV_{pp} and 280 ps pulse duration is obtained. The positive and negative parts of the GMP is also well balanced (B/A>98%) and has also good symmetry in shape. The low ringing level (C/(A+B)<10%) of –20.2 dB is obtained. The measured frequency spectrum as shown in Fig. 5 shows that the GMP of 3.6 GHz center frequency (f_c) and power of –64.25 dBm (< FCC limit (-41dBm) in frequency band of 3.1 GHz-10.6 GHz) is obtained. The voltage sensitivity of GMP as shown in Fig. 6 depicts that ± 5 % variation of V_{dd} (1.8V) changes f_c (3.6 GHz) by 5 to 6% due to the changing of rising and falling time of MOS transistor with V_{dd}. The GMP repetition

rate is 1.16 GHz. The transmitted signal is measured after source follower by using SS probe and balun. The measured transmitted signal and its spectrum as shown in Figs. 7 and 8 depict that the transmitted GMP duration and its center frequency change to 0.46 ns and 2.33 GHz, respectively, due to SIDO and amplifier's output capacitance and resistance. Fig. 9 shows the received signal which is the differentiated form of transmitted GMP but with the same pulse width (0.46ns). Fig. 10 shows 3.5 GHz center frequency of the received signal which is slightly higher than that of the 1.41 times of the transmitted signal (2.33GHz) as computed. The transmitted and received pulse repetition rate are to be the same as 1.16 GHz. The transmission loss is found to be -24 dB at 2.33 GHz from transmitted and received power. Fig. 11 shows the received signal periodic jitter after off chip amplifier where the standard deviation (σ) is 3.38 ps. Total power dissipation is 21.6mW at 1.8 V.

4. Measurements of On-chip Integrated Antennas

A wafer level measurement set-up for scattering parameter (S-parameter) in the frequency domain is shown in Fig. 12. It consists of HP8510C vector network analyzer, 180° hybrid couplers (KRYTAR; 6-26.5 GHz), probe station and signal-signal (SS) probes. From measured S-parameters, reflection coefficient (S_{11}) and transmission coefficient (S_{21}) were investigated in the frequency domain. Figure 13 shows a measurement set-up for UWB signal transmission. It is composed of Agilent N4902B serial bit error rate tester (BERT), two impulse forming networks (IFNs, Picosecond), and Agilent 86100C sampling oscilloscope. Figure 14 shows a sample structure for the measurement of signal transmission characteristics through stacked Si chips using integrated dipole antennas. Number of the inserted Si chips between transmitting and receiving antennas was changed from 0 to 10. Thickness of Si chip is 0.26 mm per chip, so that line-of-sight (LOS) distance between transceiver antennas changed from 3.01 to 4.14 mm.

Figures 15(a) and 15(b) show dependence of the number of inserted Si chips on transmission gain at the frequency of 20 GHz and received peak-to-peak voltage of Gaussian monocycle pulse. Propagation loss decreased from –1.3 dB/chip to –0.14 dB/chip by increasing the resistiviety of inserted Si chips from 10 to 2290 Ω·cm for 20 GHz sinusoidal wave propagation. Propagation loss of received peak-to-peak voltage also improved from –0.08 mV/chip to –0.03 mV/chip by inserting high resistivity Si chips.

5. Equivalent Circuit Model for Si Integrated Antennas

An equivalent circuit model of Si on-chip dipole antenna including transmission media for CMOS integrated circuits was developed to analyze the UWB transmission characteristics in ULSI chips. Figure 16 shows the proposed equivalent circuit model. Transmitting and receiving antennas consisted of RLC (R_{rad}, C_{ant}, and L_{ant}) series resonant circuits and they were fabricated on Si chips, so that parasitic components (C_{SiO2}, R_{Si}, C_{Si}, and $C_{low\text{-}k}$) were added. Signal propagation channel was modeled as a transmission line (R, L, R_{sub}, and C_{sub}). Parameter fittings of equivalent circuit model were carried out using Agilent advanced design system (ADS). Figures 17(a) and 17(b) show comparison of the simulation of equivalent circuit model with the measurement on S_{11} and S_{21}, respectively. The simulation results using the equivalent circuit model fitted well with the measurement data of S_{11} and S_{21}. Using extracted RLC parameters, received waveform of Gaussian monocycle pulse was simulated by HSPICE circuit simulator in time domain as shown in Fig. 18. The simulation result could reproduce the measurement data.

6. Conclusion

Generation of ultra short GMP using 0.18 μm CMOS technology was demonstrated for the first time. The transmission and reception of generated GMP at the rate of 1.16 Gbps by meander dipole antenna integrated on the same Si chip were also demonstrated successfully .

Wireless signal transmission through stacked Si chips using on-chip integrated antennas was demonstrated. Equivalent circuit model was developed for Si on-chip integrated antennas and RLC parameters were extracted to reproduce received signal waveform of GMP by HSPICE circuit simulator.

References

[1] T. Kikkawa, S. Chikaki, R. Yagi, M. Shimoyama, Shishida, N. Fujii, K. Kohmura, H. Tanaka, T. Nakayama, S. Hishiya, T. Ono, T. Yamanishi, A. Ishikawa, H. Matsuo, Y. Seino, N. Hata, T. Yoshino, S. Takada, J. Kawahara, K. Kinoshita, "Advanced Scalable Ultralow-k/Cu interconnect Technology for 32nm CMOS ULSI Using Self-Assembled Porous Silica and Self-Aligned CoWP Barrier", in *IEEE International Electron Devices Meeting Technical Digest,* Washington DC, Dec.5, 2005, pp.99-102.

[2] A. Iwata, M. Sasaki, T. Kikkawa, S. Kameda, H. Ando, K. Kimoto, D. Arizono, and H. Sunami, "A 3D Integration Scheme utilizing Wireless Interconnections for Implementing Hyper Brains", in *IEEE International Solid-State Circuits Conference Technical Digest,* San Francisco, CA, Feb., 2005, pp.262-263,

[3] B. A. Floyd, C. M. Hung, and Kenneth K. O, "A 15-GHz Wireless Interconnect Implemented in a 0.18-μm CMOS Technology Using Integrated Transmitters, Receivers, and Antennas," *IEEE J. Solid-State Circuits*, vol.37, no.5, pp.543-552, May 2002.

[4] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "High Transmission Gain Integrated Antenna on Extremely High Resistivity Si for ULSI Wireless Interconnect", *IEEE Electron Device Letters*, Vol. 23, No.12, December 2002, pp.731-733.

[5] S. Watanabe, A. B. M. H. Rashid, and T. Kikkawa, "Effect of High Resistivity Si substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects," Japanese Journal of Applied Physics, Vol.43, No.4B, pp.2297-2301, Apr. 2004.

[6] T. Kikkawa, K. Kimoto and S. Watanabe, "Ultrawideband characteristics of fractal dipole antennas integrated on Si for ULSI wireless interconnects", *IEEE Electron Device Letters*, Vol. 26, Issue 10, Oct. 2005, pp.767 - 769.

[7] K.K. O, K. Kim, B.A. ; Floyd, J.L. Mehta, H. Yoon; C.M. Hung, D. Bravo, T.O. Dickson, X. Guo, R. Li, N. Trichy, J. Caserta, W.R. Bomstad, J. Branch, D.J. Yang, J. Bohorquez, E. Seok, L. Gao, A. Sugavanam, J.J. Lin, J. Chen, and J.E. Brewer," On-chip antennas in silicon ICs and their application," *IEEE Trans. on Electron Device*s, Vol. 52, Issue 7, July 2005, pp.1312 - 1323.

[8] K. Kimoto and T. Kikkawa, "Transmission Characteristics of Gaussian Monocycle Pulses for Inter-Chip Wireless Interconnections Using Integrated Antennas", Japanese Journal of Applied Physics Vol. 44, No. 4B, 2005, pp.2756-2760

[9] P.K. Saha, N. Sasaki and T. Kikkawa, "A Single Chip Gaussian Monocycle Pulse Transmitter using 0.18 um CMOS Technology for Intra/Inter-chip UWB Communication", *in Digest of Technical Papers, IEEE Symposium on VLSI Circuits*, Honolulu, HI, June 11-15, 2006, pp.252-253.

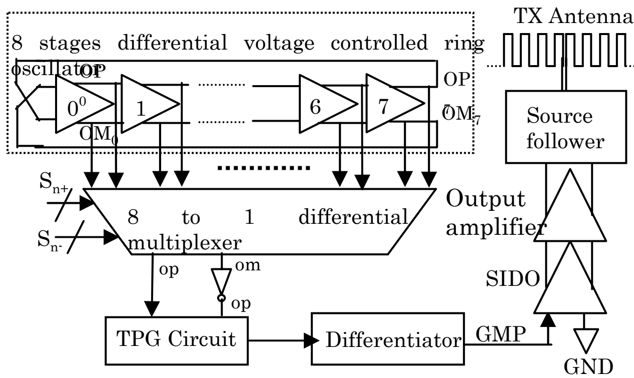


Fig. 1 GMP transmitter circuit schematic diagram.

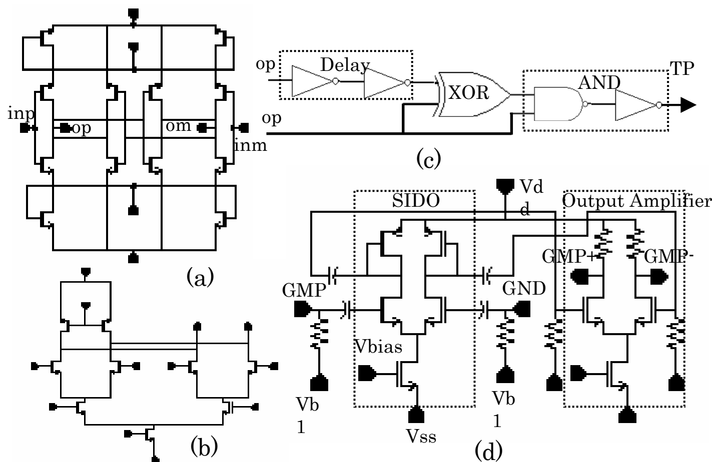


Fig. 2 Building blocks. (a) VCO differential delay cell. (b) 2 to 1 differential multiplexer. (c) TPG circuit. (d) SIDO and output amplifier.

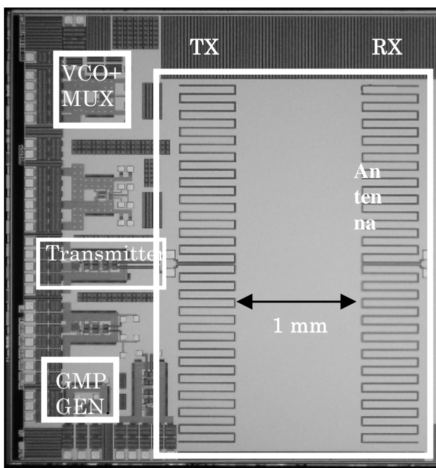


Fig. 3 Chip die microphotograph.

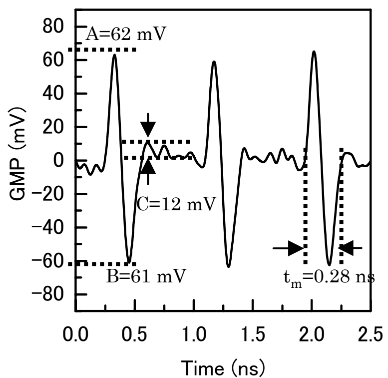


Fig. 4 Measured GMP signal before single input dual output amplifier.

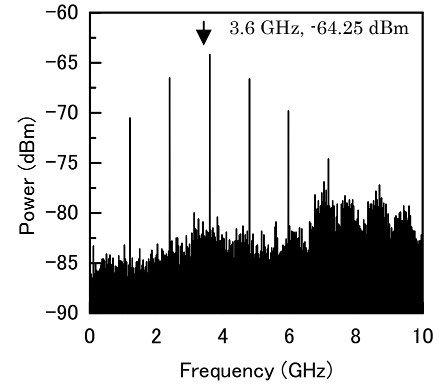


Fig. 5 Measured spectrum of GMP.

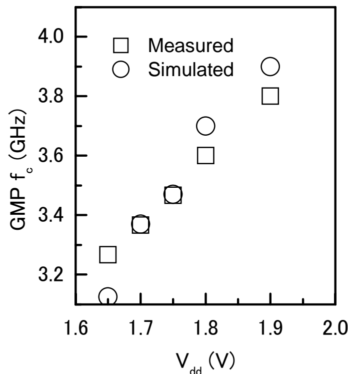


Fig. 6 V_{dd} sensitivity of GMP center frequency (f_c).

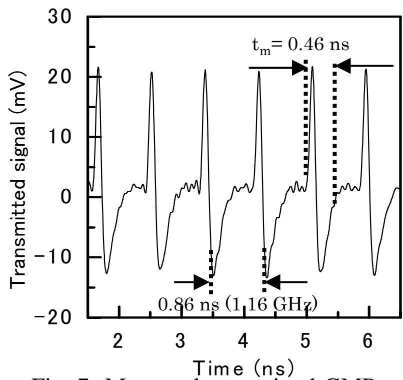


Fig. 7 Measured transmitted GMP at TX antenna pad after source follower.

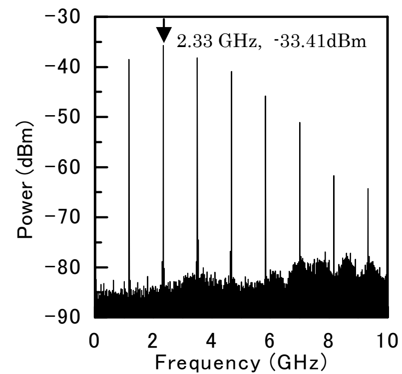


Fig. 8 Frequency spectrum of the transmitted signal.

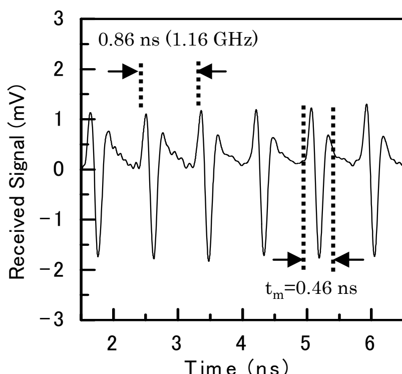


Fig. 9 Measured received signal at the receiving antenna.

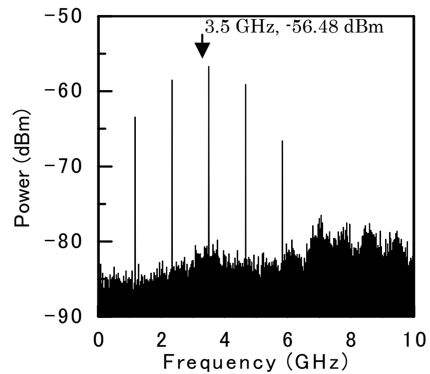


Fig. 10 Frequency spectrum of the received signal.

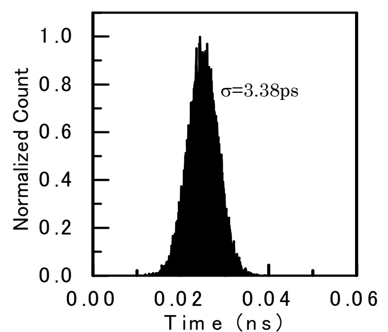


Fig. 11 Received signal periodic jitter.

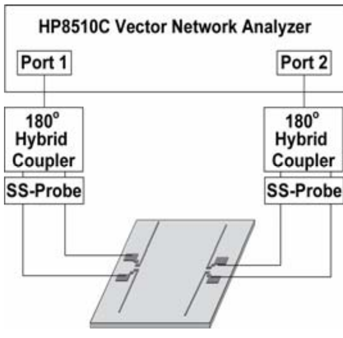


Fig. 12. Measurement set-up for antenna characteristics in frequency domain.

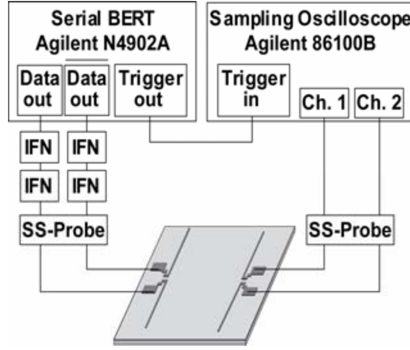


Fig. 13. Measurement set-up for UWB signal transmission characteristics in time domain.
IFN : Impulse Forming Network

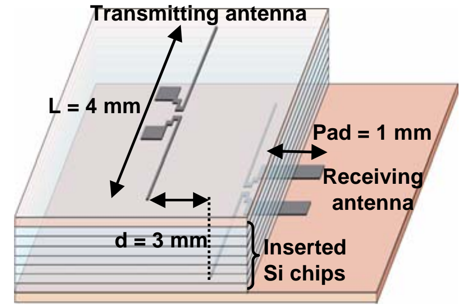
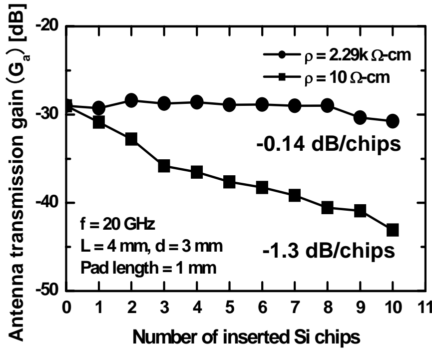


Fig. 14. Measurement sample for signal transmission through stacked Si chips (antenna length (L) = 4 mm, horizontal separated distance (d) = 3 mm, and pad length = 1 mm).



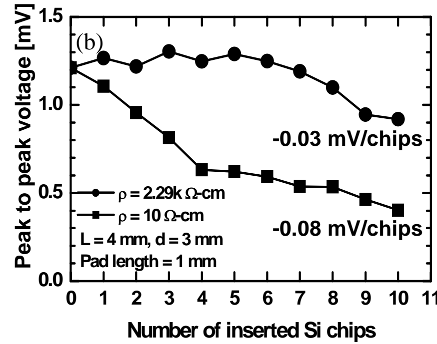


Fig. 15. Dependence of the number of inserted Si chips with resistivity of 10 and 2290 Ω·cm (a) antenna transmission gain at 20 GHz frequency, (b) received Gaussian monocycle pulse peak-to-peak voltage.

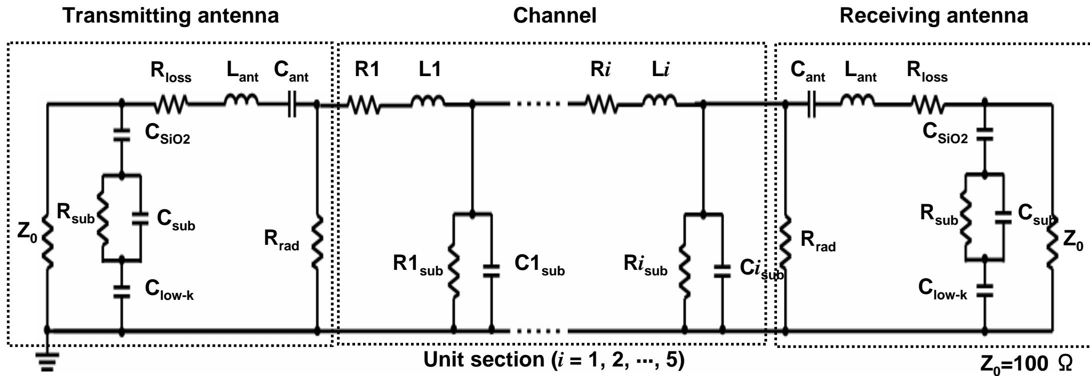
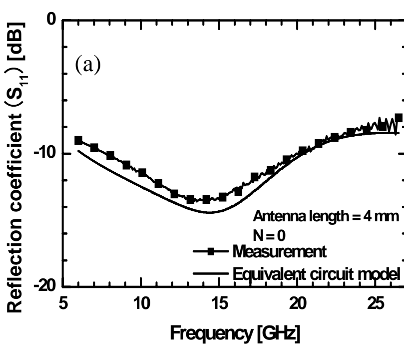


Fig. 16. Equivalent circuit model of Si integrated antennas including signal propagation channel (Z_0: characteristic impedance).



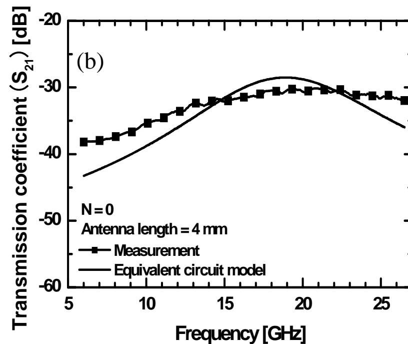


Fig. 17. Comparison of simulation using equivalent circuit model with measurement for stacked Si chip (a) reflection coefficient (S_{11}), (b) transmission coefficient (S_{21}).

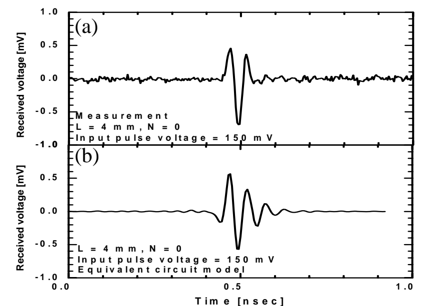


Fig. 18. Comparison between measurent and equivalent circuit model for received GMP.
(a) Measurement. (b) Equivalent circuit model.