Development of Reliable High-k Gate Dielectrics for Scaled MOSFETs

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Outline

- Introduction
- Reliability study

  Static bias temperature instability in plasma nitrided SiON gate dielectrics

  Bias temperature instability under high-frequency bipolar gate bias stressing in plasma nitrided SiON gate dielectrics
- Practical application of ALD Si nitride
- Development of ALD high-k gate dielectrics
- Summary

Introduction

For realization of 3 dimensional-custom stack system, we need high-performance transistors.

To fabricate such transistors, one of the key issues is development of high reliable gate dielectrics.

For the development, the following subjects were studied in our group:

- Reliability study
- Practical application of ALD Si nitride
- Development of ALD high-k gate dielectrics

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background

Remaining problems

- Detail mechanism of negative BTI (NBTI) has still not fully been understood for SiON gate dielectrics.
- For plasma-nitrided gate dielectrics, quantitative impact of nitrogen concentration on NBTI has not been reported yet.

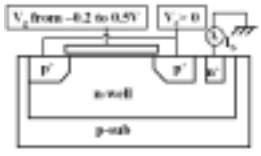
To examine the above,

- Separate evaluation of the effect of ΔN_{it} and ΔN_{ot} to NBTI is extremely important.

Experimental details -1:

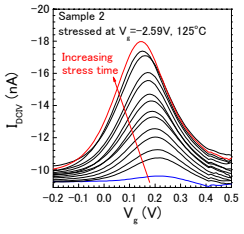
Measurement:

For the separation, modified **DCIV** measurements were used.



◯ Interface trap generation ΔN_{it} is calculated from the DCIV peak height.

◯ Fixed oxide charge buildup ΔN_{ot} is obtained from the shift of DCIV peak.



Experimental details -2:

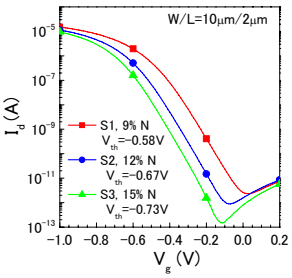
Devices:

pMOSFETs with p^+ poly-Si gate, plasma-nitrided SiON gate dielectric.

W/L=10 μm/2 μm.

T_{ox}=2.0nm, N% = 9, 12, 15%,

EOT= 2.22, 2.17, 2.12 nm

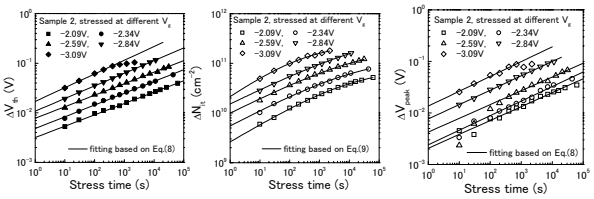


Stress:

negative V_g, at 125°C

other electrodes grounded

Results and discussion: Time evolutions of ΔV_{th}, ΔN_{it} and ΔV_{peak}



ΔV_{th} has a power- law dependence on stress time as shown by these linearly fitting curves.

Corresponding ΔN_{it} follows the power-law dependence only at the earlier stress time. With increasing stress time, the slope continues decreasing due to the finite Si-H number.

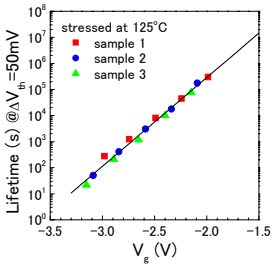
Corresponding ΔN_{ot} is much smaller than that predicted by the power-law dependence at earlier stress time. With increasing stress time, ΔN_{ot} follows the power-law dependence.

In the early stage of stress, main contribution to ΔV_{th} is ΔN_{it}. With increasing stress time, the relative contribution of ΔN_{ot} increases.

Results and discussion:

Nitrogen concentration dependence on lifetime

N% = 9, 12, 15%



Contrary to our expectation, the lifetime found to be almost independent of N%.

Since the nitrogen-induced NBTI is mainly induced by interface nitrogen, the absence of nitrogen dependence is due to the fact that peak nitrogen concentration is around the upper half of the dielectrics.

Therefore, the nitrogen concentration in the plasma-nitrided SiON layer can be further increased without sacrificing the NBTI lifetime, which leads to a superior suppression ability of boron penetration.

Conclusions:

- ΔN_{it} and ΔN_{ot} can be monitored by the modified DCIV method separately for ultrathin MOSFETs.
- During the NBT stress, ΔN_{ot} is not linearly related to ΔN_{it}.
- Plasma nitridation was found to be a superior method to fabricate the SiON gate dielectric in the viewpoint of NBTI reliability and suppression of boron penetration.

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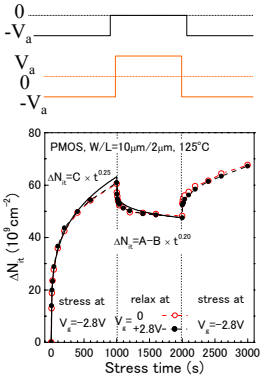
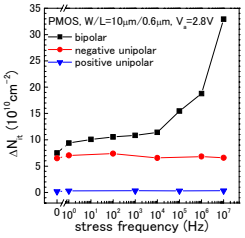
Introduction-1:

- For pMOSFET under **static** NBT stress, it has been known that devices were degraded at the $V_g = -V_a$ stage, and was partially recovered at the $V_g = 0$ or $V_g = +V_a$ stage.
- This implies that the dynamic NBT stress may have the similar degradation with the unipolar NBT stress regardless of stress frequency.



Introduction-2:



- Indeed, under unipolar BT stress, the degradation is almost independent of frequency.
- However, under bipolar BT stress, the degradation is **enhanced** at f > 10 kHz, and is dependent of frequency.

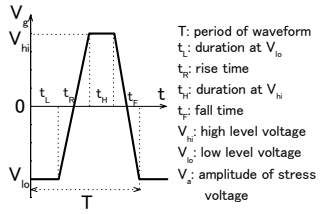
Experimental details:

Devices:

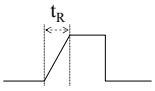
pMOSFETs with p^+ poly-Si gate and plasma-nitrided SiON gate dielectrics. T_{ox}=2.0nm, N% = 15%, EOT= 2.12 nm

Stress:

To reveal the degradation enhancement mechanism more clearly, stress pulse wave dependence on the degradation was studied in bipolar BTstress.



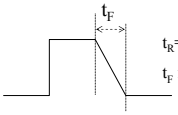
Experimental results:



t_F=5.5ns,

t_R from 5.5ns to 99.9ns.

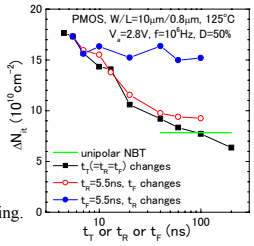
• The enhancement almost keeps the same.

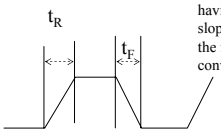


t_R=5.5ns,

t_F from 5.5ns to 99.9ns.

• The enhancement decreases with t_F increasing.

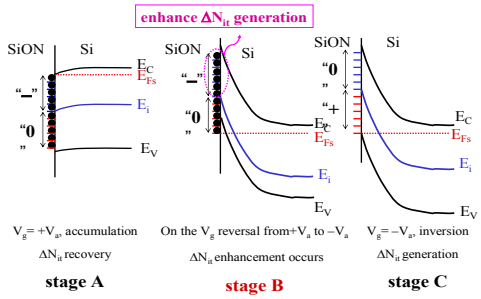




having the same slope with that in the following conventional case: $t_T = t_R = t_F$ from 5.5ns to 99.9ns.

This clearly suggests that ΔN_{it} enhancement under bipolar BT is mainly due to the rapid voltage transition from positive to negative.

Model and discussion-1:



"–": negatively charged; "**0**": neutral; "+": positively charged

Stage B is the transient state. Since the emission rate of trapped electrons from the interface is finate, if the gate voltage shifts from positive to negative so quickly that the emission of the trapped electrons cannot follow the voltage.

Model and discussion-2:

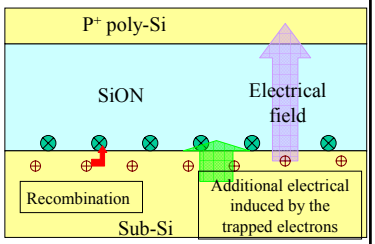
NBTI degradation:

$Si_3{\equiv}Si\text{-}H + h^+ \leftrightarrow Si_3{\equiv}Si\bullet + X_{interface}$

In the stage of B, $V_g < 0$

The **transient trapped electrons** in the interface states:

- Additional build-in electrical field.
- In the Si channel side, the direction of this field is the same as that provided by the following negative gate bias.



The reaction is enhanced.

Conclusions:

- For pMOSFET under dynamic BT stress, besides the degradation at the V_g = -V_a stage and recovery at the V_g = +V_a stage, an **additional** degradation occurs at the falling edge of each cycle.
- The additional degradation is proposed to arise from **the trapped electrons** in the transient states upon V_g switching from +V_a to –V_a quickly.
- For reliability improvement in high frequency (such as VHF) CMOS logic operation, this waveform effect may need to be taken into account.

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Application of ALD Si nitride/SiO_2 gate dielectrics to future DRAMs

- Plasma-nitrided SiO_2 has been proposed as the gate dielectrics for next-generation DRAMs.

Problems

1. With scaling T_{ox}, the low nitrogen concentration

   ↓ Heavy thermal budget peculiar to DRAM fabrication process

   Insufficient suppression of boron penetration

2. High nitrogen concentration → Degrade NBTI

New gate dielectrics for future DRAMs are desired.

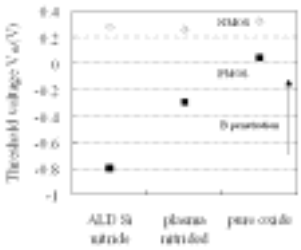
Purpose

- We have developed ALD Si nitride/SiO_2 stack gate dielectrics.
  - Merits
    - High suppression ability of boron penetration
    - Excellent reliability characteristics such as soft breakdown free phenomena

↓

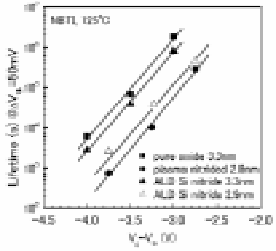
We applied the stack gate dielectrics to future DRAMs.

Suppression of boron penetration after high thermal budget



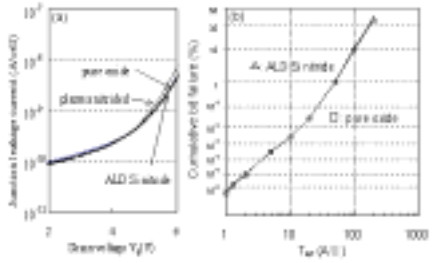
Since there is smallest V_{th} shift for ALD stack gate dielectrics, the stack dielectrics have a special advantage over plasma-nitrided gate SiO_2 and pure gate oxide as regards the suppression of boron penetration.

NBTI characteristics



- ALD stack gate dielectrics exhibit only slightly worse NBTI characteristics than pure oxide.
- Better NBTI characteristics were achieved than those of plasma-nitrided gate SiO_2.

Memory-cell characteristics



- ALD stack gate dielectrics show identical junction leakage current to that of pure gate oxide and better characteristics than the plasma-nitrided gate SiO_2.
- MCs having transistors with ALD stack dielectrics show identical T_{ref} distribution to those having transistors with pure gate oxide.

Conclusions:

・ALD stack dielectrics are a promising candidate for gate dielectrics of future high-speed and high-reliability DRAMs.

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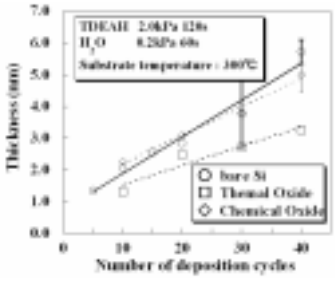
- HfO_2 is one of the most promising candidates for future gate dielectrics owing to its high dielectric constant and high thermal stability in contact with Si.
- To date, for ALD of HfO_2, the most frequently used precursor combination is $HfCl_2$ and H_2O.
- There exist problems.
  - Particle adhesion due to solid source
  - Cl contamination

In this study, $Hf[N(C_2H_5)_2]_4$, tetrakis diethyl amino hafnium (TDEAH) and H_2O was used as source gases for ALD.

Dependence of HfO_2 thickness on number of deposition cycle on Si or SiO_2

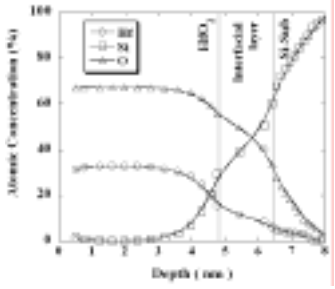


The thickness varies almost linearly with cycle number.

From the slope, the deposition rate was estimated to be 0.06- 0.1 nm

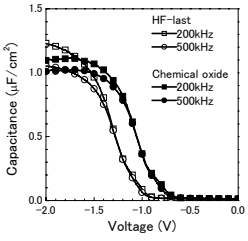
The film growth follows a layer-by-layer growth kinetics.

High-resolution RBS profile



The ratio of Hf and O is 1:2, indicating that almost stoichiometric HfO_2 was obtained.

C-V characteristics

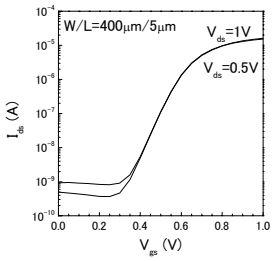


No hysteresis was observed for both HfO_2 on Si and on chemical SiO_2.

The κ-value of the ALD HfO_2 was estimated to be 12-14.

Fixed charge density of 3.6×10^{12} cm^{-2} on Si and -5.7×10^{11} cm^{-2} on chemical oxide.

I_d-V_g characteristics of MOSFET



NMOSFET with Al gate was fabricated using a simple one-mask process.

Good subthreshold slope of about 77 mV/dec was obtained.

Conclusions:

・ALD using TDEAH and H_2O is promising for high reliable high-k gate dielectrics.

Summary

- In reliability study, we established new evaluation method and got new information.
- We showed the applicability of ALD Si nitride/SiO_2 stack gate dieleictrics to future DRAMs.
- We established ALD of high-k gate dielectrics.

From the veiwpoints, we developed and improved gate dielectrics for high-performance transistor.