Metal Gate and Junction Technologies for Leading Edge Devices

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1. Introduction

Our COE project aims development of 3DCSS system that needs high-performance mixed-signal devices. We are working for development fundamental device technologies for such devices. Our investigation subjects are categorized to major two fields. One is shallow junction formation and another is metal-gate workfunction tuning. The former and the latter are key technologies to improve f_T and f_{MAX} by reducing parasitic source/drain resistance and gate resistance, respectively. In addition, they are core technologies for CMOS logic devices.

In this abstract, major research establishments obtained during the term of our COE project.

2. Metal gate technology

Gate depletion issue is one of the most important issues to be solved for improving MOSFET performance with scaling. Since the gate depletion is attributed to semiconducting nature of poly-Si gate, its replacement with metal material is the best way to remove the problem. However, it also leads to losing the benefit of workfunction tuning by doping. Since a dual gate structure is indispensable for CMOS devices, we have worked on this target for these several years [1-15].

Metal gate MOS fabrication processes are categorized to several manners, as shown in Fig.1. Mo gate are suitable for conventional self-aligned gate process and replacement gate process. We have reported workfunction tuning with nitrogen incorporation into Mo [1-5]. Though workfunction tunable range was not enough for practical device application, we have indicated nitrogen pileup at the Mo/gate SiO_2 interface was a key to modulate workfunction value.

FUSI (Fully Silicided) gate process [6,7] that converts entire part of gate poly-Si to silicide by slicidation reaction, as shown in Fig. 1, is also a workfunction tuning method. Impurities introduced to poly-Si prior to the silicidation are swept out towards the gate insulator interface during the silicidation and form pileup a the interface. We have investigated the relationship between silicidation condition of NiSi FUSI gate and its workfunction [8-10]. As shown in Fig. 2, Sb pileup peak height strongly depended on the FUSI process temperature. Though motive force of Sb redistribution is segregation at the silicide/poly-Si interface, too fast silicidation at high temperature (500°C) silicidation resulted in insufficient pileup formation for workfunction modulation. Such a process condition dependence is considered to be the origin of discrepancy of workfunction tunable range between research organizations shown in Fig. 3.

Precise location of Sb pileup was evaluated by XPS measurement [11] utilizing the feature that Sb doped specimen was cleavable at the gate oxide, as shown in Fig. 4(a). The specimen was divided to upper and lower parts, as shown in Fig. 4(b). Sb-O related signals were observed for both the upper and the lower specimens. However, other specimens which were fabricated by different conditions showed no Sb penetration [12], in spite that both specimens showed workfunction shift. This discrepancy is another example of process sensitivity of FUSI process, and it also shows workfunction shift mechanism is still an open question.

Although NiSi is the most popular material for FUSI process, we are also working on Pd_2Si as an alternative candidate. Lower silicidation temperature of Pd_2Si gives flexibility to device fabrication process, and higher thermal stability is also advantageous. Defect formation during FUSI process is one of the critical issues that blocks FUSI gate against practical use [8,9,11]. We have discussed slicidation mechanism of Pd_2Si based on silicidation with three kinds of heating apparatuses [13-15]. It was concluded that low temperature silicidation led to defective film formation because of Si diffusion, as shown in Fig. 5. We believe that this tendency is common for NiSi FUSI. Therefore high ramp-up apparatus should be used for FUSI gate formation. It should be also noted that workfunction shift direction in Pd_2Si by impurity pileup formation is quite opposite to NiSi and PtSi cases, as shown in Fig. 3. Interface structure of Pd_2Si should be characterized by photoelectron spectroscopy like a NiSi case shown above for the discussion of workfunction shift mechanism.

3. Shallow Junction formation by laser annealing

Currently introduction of new generation annealing

technologies that succeed RTP are demanded for source and drain (S/D) formation of leading edge device mass production. New annealing technologies provide shallower S/D necessary for further scaling of CMOS devices. Melt laser annealing (LA) is one of such technologies. We have investigated the melt LA using KrF excimer laser [16-22,27] and solid state green laser [23-26] as a light source to heat up specimens. Among the achievements obtained through these works, proposal of partial-melt LA (PMLA) is the most notable one.

The words “melt LA” currently stand for LA that utilizes melting point difference between crystalline Si and amorphous Si. Selective melting of a thin amorphous Si layer whose melting point is lower than crystalline by about 300°C suppresses over-melt to crystalline Si and leads to high activation due to non-equilibrium re-crystallization. Ge^{+} implantation prior to dopant implantation is usually used for the a-Si layer formation.

We have proposed the combination of substrate heating and LA, that is heat-assisted LA (HALA) [16-18]. Although this method reduced necessary laser energy density to obtain good dopant activation, basic idea is common to the ordinary melt LA. We have added solid-phase regrowth process prior to laser irradiation. It was the proposed new LA scheme, that is, PMLA. By performing pre-annealing for appropriate duration, amorphous layer thinner than initial thickness can be obtained, as shown in Fig. 6. The a-Si thinning enbales melting shallower than initial a-Si depth, as shown in Fig. 7. PMLA is usable together with HALA. By this, PMLA obtain features which are preferable to shallow junction formation, as shown in Table I. We have demonstrated PMLA with 10-nm B-doped junction formation [20,21]. Sheet resistance about 700Ω/sq. was obtained for 10 nm junctions with negligible diffusion, as shown in Fig. 8. Please note that Fig. 8 was plotted in a linear scale to emphasis redistribution of B.

We have mainly investigated annealing method without combining it with device fabrication processes. However, introduction of new process to fabrication flow is often suffered by difficulties. In the case of LA, gate electrode deformation in isolation region, shown in Fig. 9, is typical one. To overcome such a issue, thermal diffusion analysis of annealing process should be utilized in addition to experimental approach [22,25,27].

4. Summary

Notable topics on workfunction tunable metal gate technology and melt LA technologies obtained through our COE project are summarized. Each of these technology has long research history. However, both technologies still have a lot of issues to be solved before practical use. Therefore, trial to brush up technologies and explain process mechanisms should be continued.

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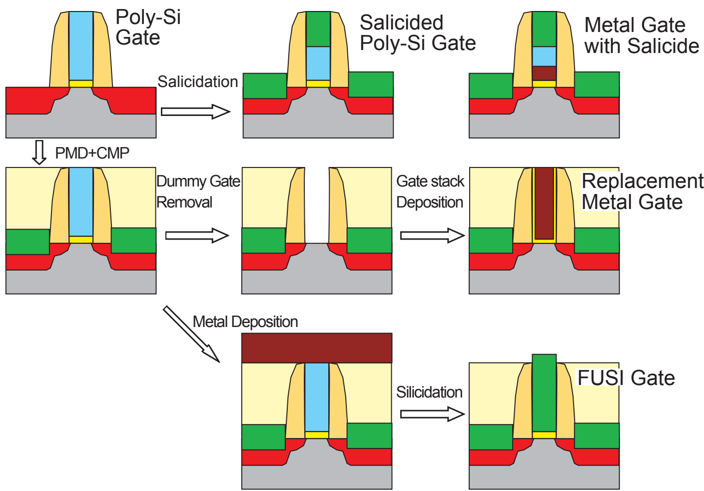

Fig. 1 Fabrication process flow and schematic cross section of MOSFETs for various gate materials.

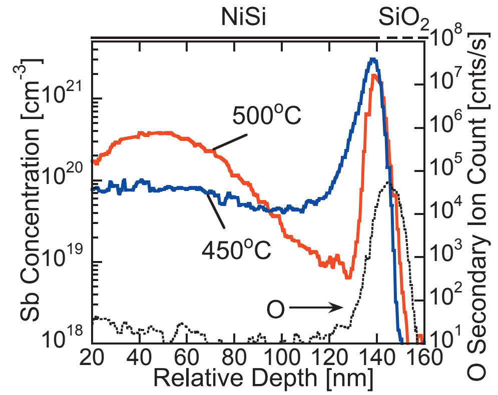

Fig. 2 Sb depth profiles in NiSi/SiO_2/Si MOS structures.

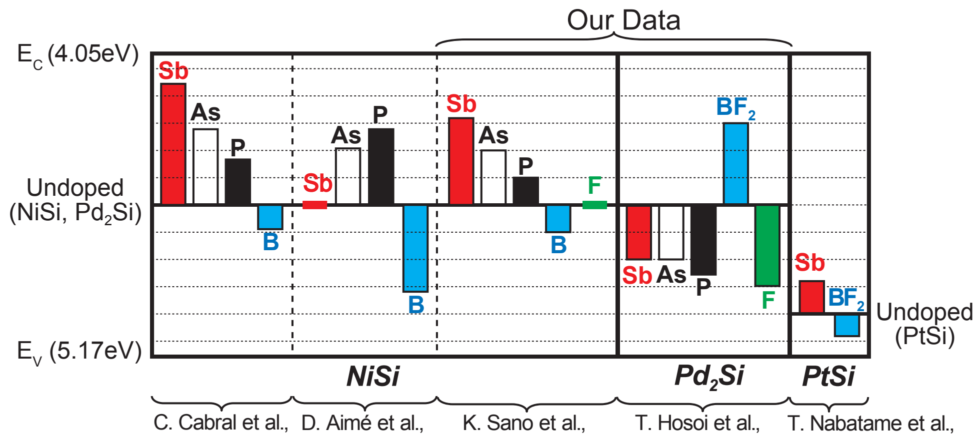

Fig. 3 Summary of the workfunction shift with various impurities in NiSi, PtSi, and Pd_2Si FUSI gate MOS structures.

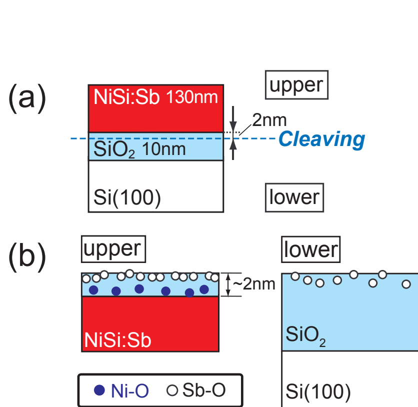

Fig. 4 (a) Sample structure for XPS measurement shown in Fig. 8. The specimen was cleaved and divided to upper and lower pieces. (b) A model to show the location of Sb pileup.

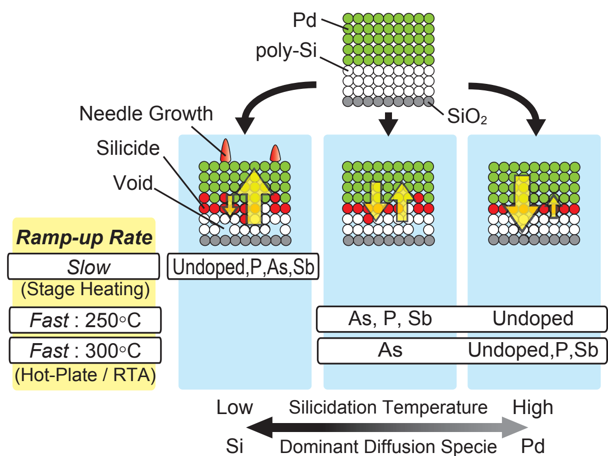

Fig. 5 Schematic model of silicide formation under various silicidation conditions. Silicidation temperature, its ramp-up rate and the presence of impurities affect the kinetics of silicide formation due to the change of dominant diffusion species.

Table I. Comparison of features for various laser annealing schemes.

Method	Laser Energy Density	Sheet Resistance	Junction Depth
Melt	High	Low	> as I.I.
non-Melt	Low	High	~ as I.I.
Partially-Melt	High	?	~ as I.I.
Partially-Melt+HA	Low	Low	~ as I.I.

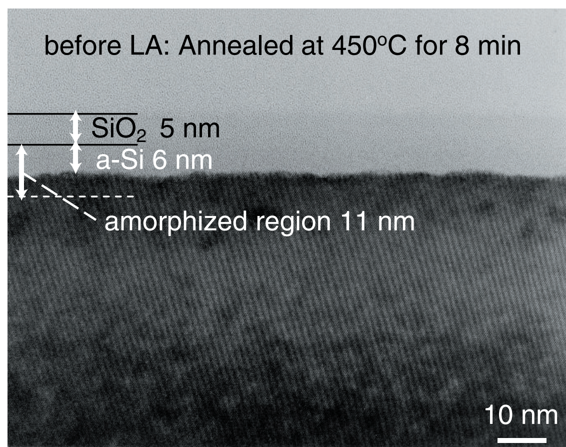

Fig. 6 XTEM image before laser irradiation. The specimen was heated for 8 min. Lower half of amorphized layer recrystallized by the heating.

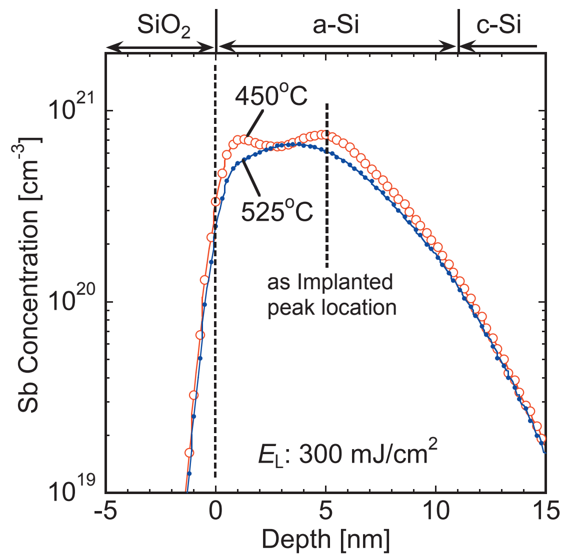

Fig. 7 Sb depth profiles after HALA. The profiles for the heat-assist of 450°C shows two peaks because of partial melting of amorphized region. Profile for 525oC was considered to be a result of non-melt LA because of absence of a-Si layer due to faster re-crystallization rate at higher temperature.

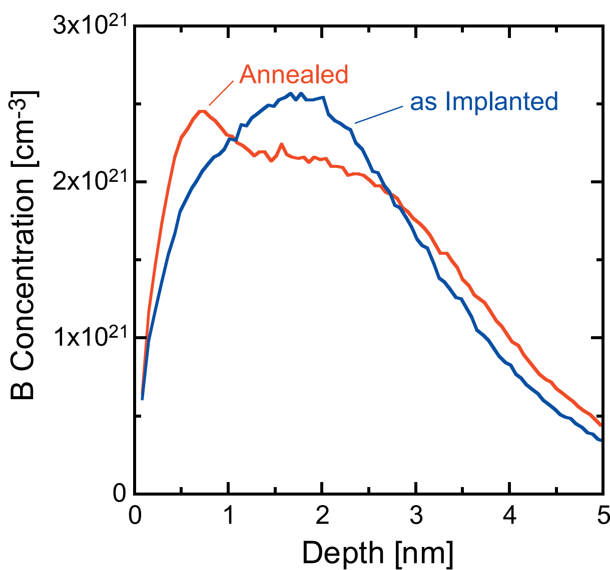

Fig. 8 B profiles before and after PMLA with heat-assist at 450°C. Diffusion in a tail region is much smaller than 1 nm.

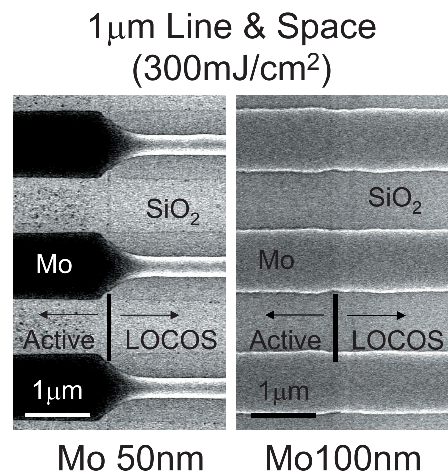

Fig. 9 Plan-view SEM microphotographs of Mo L/S formed on the border of active and isolation regions. Thin 50 nm Mo showed serious deformation.