Metal Gate and Junction Technologies for Leading Edge Devices

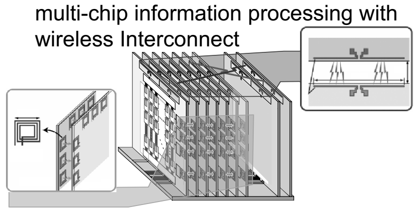
Kentaro Shibahara

Research Center for Nanodevices and Systems, Hiroshima Univ.

Fundamental Device Technologies for 3DCSS

3DCSS System

multi-chip information processing with wireless Interconnect



Tera-bit processing → high RF performance devices

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

Parasitic series resistance should be low
→ Low resistive junction formation
→ Laser Annealing

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{gd} R_g}}$$

Gate resistance should be low
→ Metal gate

Order of Presentation

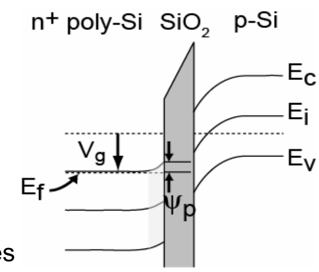
Looking back the following 5 years activities for our COE Pj.

- Metal Gate Technology
- Shallow Junction Formation

Why metal gate?: Basic expectation

- Recover EOT loss due to gate depletion.
  I_{on} vs J_g trade-off
- Lower resistivity
  RF application f_{max}

However, worfunction appropriate to CMOS devices are needed.



~ 0.4 nm
(gate dope : 1×10^{20} cm^{-3})

Introduction Timing of Metal Gate

Based on ITRS 2005 PIDS Table: Planar Bulk Devices

		2005	2006	2007	2008	2009	2010	2011	2012
1Metal ½ Pitch		90	78	68	59	52	45	40	36
HP	EOT	1.2	1.1	1.1	.9	.75	.65	.5	.5
	ΔEOT	.73	.74	.74	.29	.28	.27	.25	.25
LOP	EOT	1.4	1.3	1.2	1.1	1.0	.9	.9	.9
	ΔEOT	.65	.65	.64	.32	.32	.32	.32	.32
LSTP	EOT	2.1	2.0	1.9	1.6	1.5	1.4	1.4	1.3
	ΔEOT	.63	.63	.63	.33	.32	.32	.32	.31

Shifted at 2006 update

Band edge workfunction is hard to obtain.

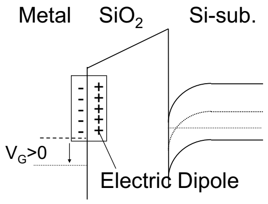
Our Target

Tunable Workfunction: Single metal gate CMOS
How?

by Pileup formation

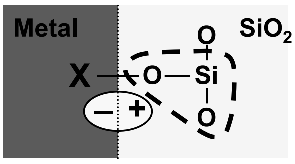
- Gate first process
  Mo + N
- FUSI (Fully Silicided) gate
  NiSi and Pd_2Si + P, As, Sb, B……

Workfunction Tuning by Pileup Formation



$$\Delta V_{FB} = -\sigma t / \varepsilon_{ox}$$

σ:Charge density
t:Distance



Electron negativity difference
→ Dipole formation

High density impurity pileup at metal/insulator interface

Dipole formation and Workfunction shift

Related Presentation

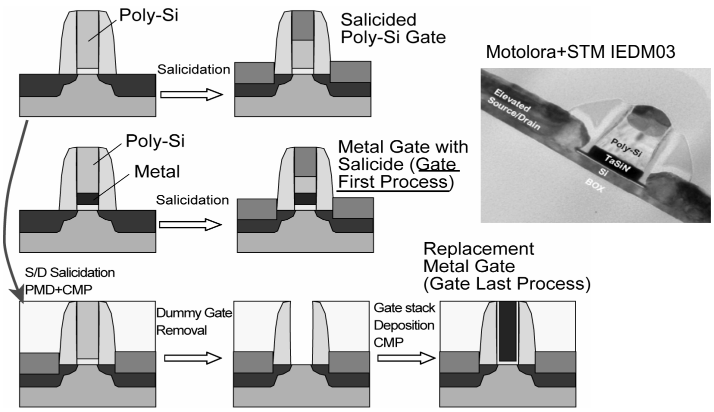
FUSI

P-18
Workfunction Tuning of NiSi and Pd_2Si Fully-Silicided Gates by Predoping
T. Hosoi, K. Sano, M. Hino, and K. Shibahara

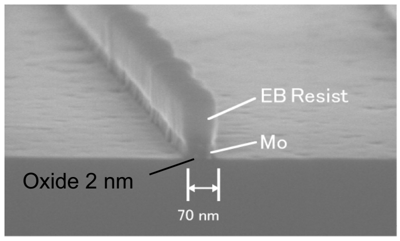
Evaluation of Chemical Structures and Work Function of NiSi near the Interface between NiSi and SiO_2
H. Murakami, H. Yoshinaga, D. Azuma, A. Ohta, Y. Munetaka, S. Higashi, S. Miyazaki, T. Aoyama, K. Hosaka, and K. Shibahara

→ First, Mo results, then FUSI briefly

Categollization: Processes for Metal/Metal Compound



Mo Fine patterning



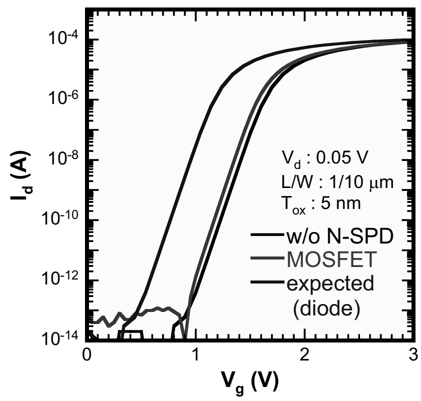
Easy Fine Patterning
High Selectivity against Oxide

→Suitable for Gate First Process
In addition, workfunction tunable

Nitrogen Solid-Phase Diffusion into Mo Gate

- p-Si (100)
- LOCOS formation
- Gate oxidation (5 nm)
- Mo & TiN sputter (50 & 30 nm) → Φ_{Mo}~ E_V
- **Nitrogen Solid-Phase Diffusion** (800°C, 1min) → Formation of N pileup $\Delta\Phi_{Mo}$~ -0.46eV
- TiN removal
- Gate formation
  - diode
  - S/D implantation (As : $5x10^{15}$ cm^{-2}, 30 keV)
  - **S/D activation annealing** (900°C, 1min)
  - Al wiring and PMA
  - MOSFET

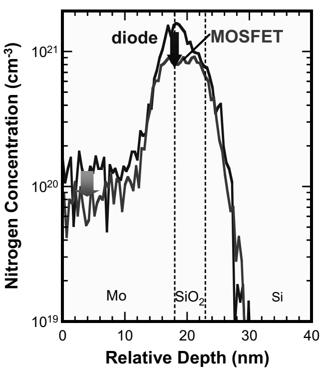
Nitrogen Solid-Phase Diffusion into Mo Gate



	$\Delta\Phi_{Mo}$
diode	-0.46 eV
MOSFET	-0.1 eV

Nitrogen Redistribution by S/D Activation Annealing

back-side SIMS



Mo-gate MOSFET

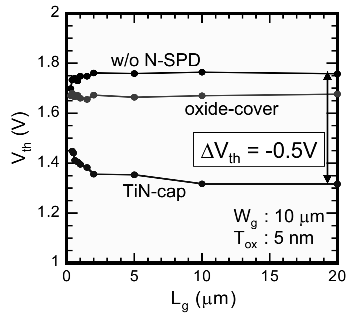
Reduction of N concentration in bulk Mo (N out-diffusion)

Pileup reduction & Reversible workfunction shift

(-0.46 eV → -0.1 eV)

Modified Process
Oxide Cover & TiN Cap

V_{th} Dependence on Gate Length

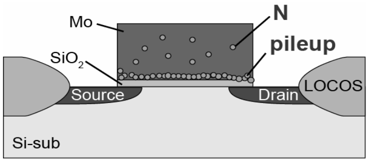


Oxide cover: ΔV_{th} ~0.15 V
TiN Cap: ΔV_{th} decreased as L_g decreased

Nitrogen Redistribution in Mo Gate (oxide-cover)

just after N-SPD

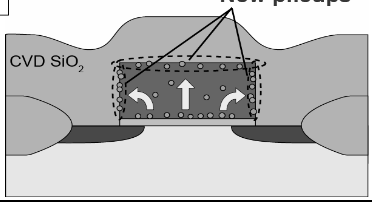
N pileup formation at Mo/SiO_2 interface



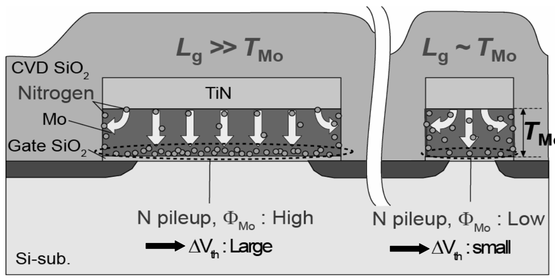
after S/D activation annealing

N pileup at bottom Mo/SiO_2 Interface redistributes to top and two side interfaces.

small V_{th} shift



Mechanism of V_{th} shift decrease (TiN-cap)



N pileups are also formed at side interfaces of Mo.

Nitrogen atoms distributed to bottom interface reduces as L_g reduced.

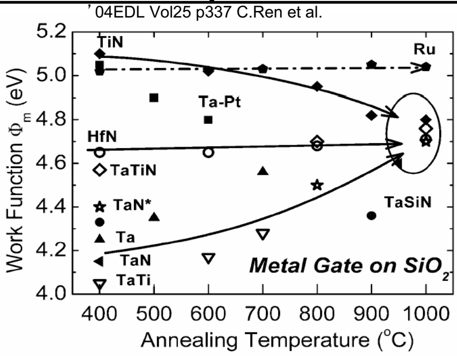
Control of Workfunction

Thus, combining Mo+N process to MOSFET fabrication process maintaining expected workfucntion value is a tough issue.

How about other metals?

Thermal Stability of Metal Workfunction

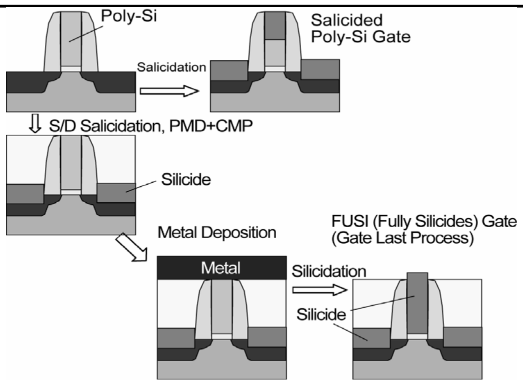
'04EDL Vol25 p337 C.Ren et al.



Important Issue for Gate First Devices.

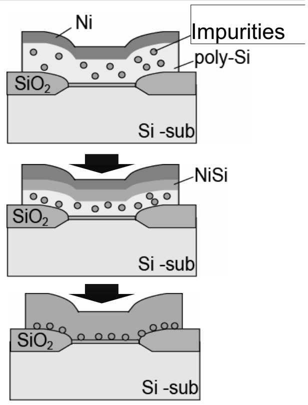
Integration scheme of dual metal is also ….

Fabrication Flow for FUSI Gate



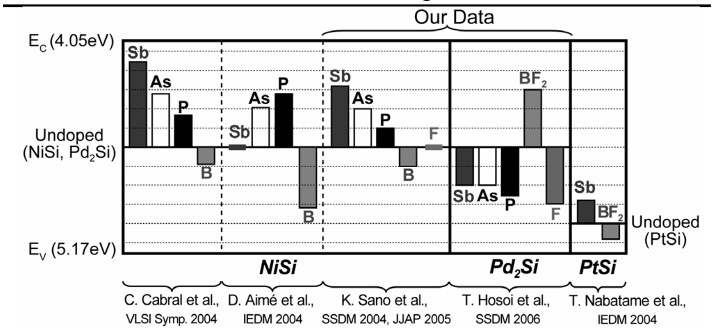
FUSI Gate MOS Diode Fabrication with Predoping

- p-Si(100)
- Gate oxidation
- Poly-Si deposition
- Gate patterning
- P, As, Sb, B …. Predoping by Ion Implantation
- Activation annealing
- Ni or Pd sputter deposition
- Full-Silicidation



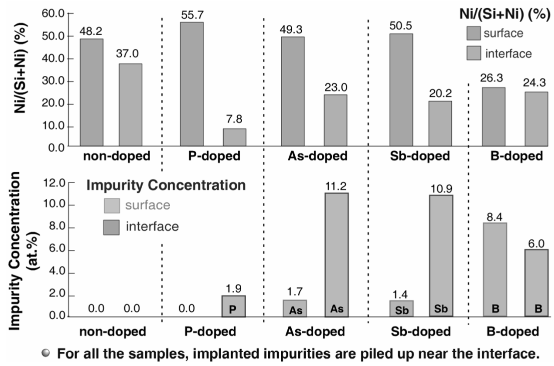
Impurities Solubility: Silicide << poly-Si
→Impurity Condensation
→Pileup formation at Oxide Interface

Workfunction Tunable Range of FUSI Gate



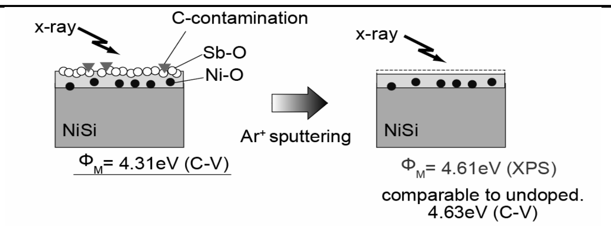
- Pd_2Si that can be processed at lower temperature provided wide workfunction tunable range.
- What is the origin of different results for NiSi?

Characterization of NiSi FUSI MOS Interface



Source: Dr. Murakami's presentation
Specimen: Made in Fujitsu

Another Characterization of NiSi FUSI MOS Interface

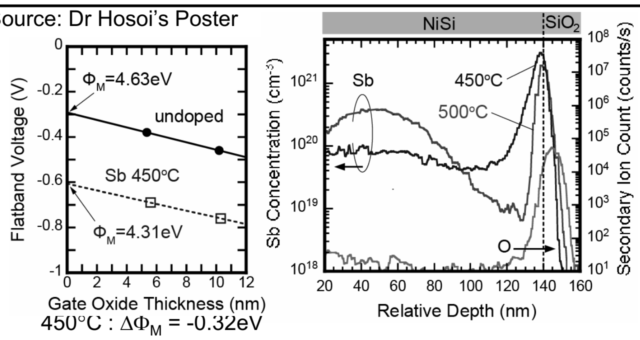


Sb-O signal was disappeared after Ar^+ sputtering necessary for workfunction evaluation.

Oxidized Sb in SiO_2 is essential for NiSi workfunction shift.
Specimen: Made in Hiroshima Univ.
← Quite different conclusion. Why?

Influcence of Process Condition on Pileup Formation

Source: Dr Hosoi's Poster

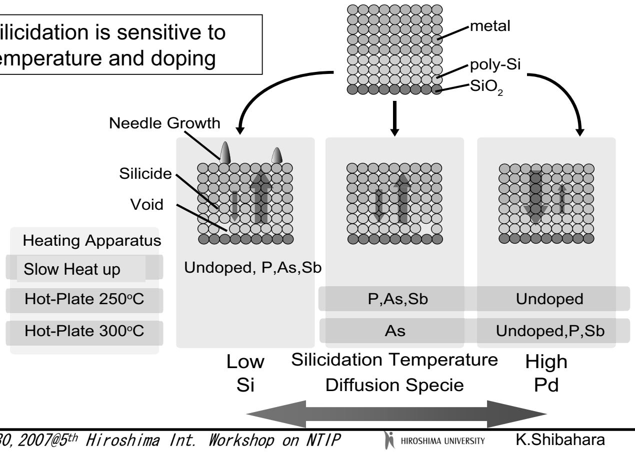


450°C : $\Delta\Phi_M$ = -0.32eV
500°C : no Φ_M shift

Pileup peak concentration : 450°C > 500°C
FUSI Workfunction Tuning: Sensitive to process condition

Influence of Temperature and Doping: Pd_2Si

Silicidation is sensitive to temperature and doping



Press Release From IBM and Intel: Metal+high-k in 2008

Jan. 27, 2007

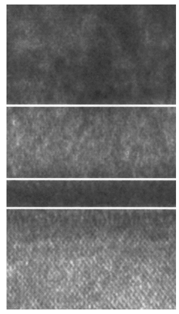
http://www-03.ibm.com/press/us/en/pressrelease/20980.wss

IBM Advancement to Spawn New Generation of Chips: "First fundamental change to basic transistor in forty years"

http://www.intel.com/pressroom/archive/releases/20070128comp.htm

Intel Transistor Technology Breakthrough Represents Biggest Change to Computer Chips In 40 Years

Intel's new gate stack ???



Even if they really ship products in 2008, research on metal gate should be continued. We have not understand well nature of the new gate stack yet.

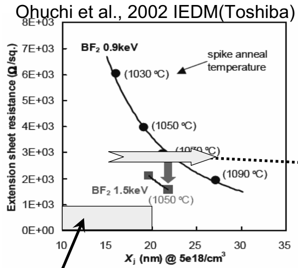
Order of Presentation

- Metal Gate Technology
- Shallow Junction Formation

"Diffusion Less"

Shallow Junction: Key Technology for MOSFET Scaling

Ohuchi et al., 2002 IEDM(Toshiba)



Optimized Spike Annealing

(sub-seconds RTA by halogen lamp heating)

X_j (Junction Depth) increase by *diffusion*

We need this range!

"*Diffusion Less*" is the key word that represents a demand for post-spike annealing technologies.

Candidates of Post-Spike Annealing

Low temperature & Long duration

Solid phase regrowth: hr-min

High temperature & Short duration

Flash lamp: ms – μs

LSA

CW Laser Annealing: ms – μs

Pulse Laser Annealing: ns

What is the best scheme for pulse laser?

Our Target

Summary of our activities on LA (Laser Annealing)

KrF Excimer Laser

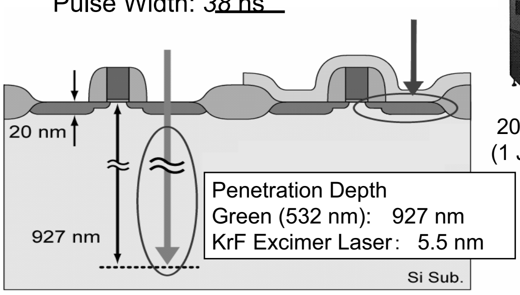
- HALA:Heat-assited LA
- PMLA: Partial Melt LA

Solid State Green Laser

- LA with light absorbing layer
- Analysis of LA with phase switch

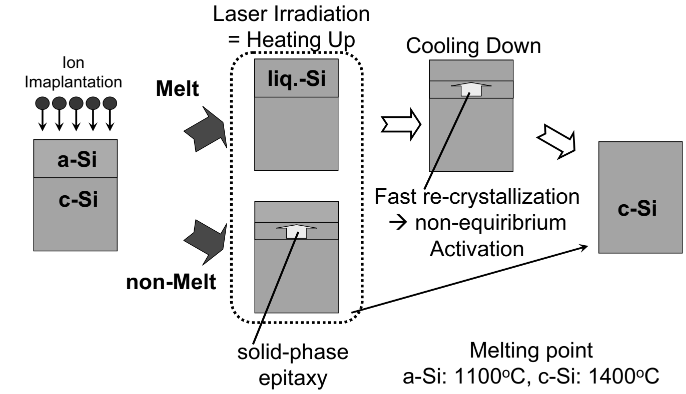
Merits of Excimer Laser

LA KrF Eximer Laser (λ: *248* nm)
Pulse Width: *38* ns



200 W **Laser**
(1 J/pulse, 200 Hz)

Schemes for Conventional Laser Annealing

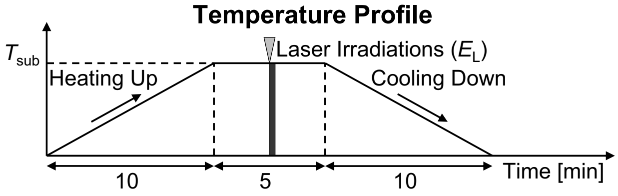


Melting point
a-Si: 1100°C, c-Si: 1400°C

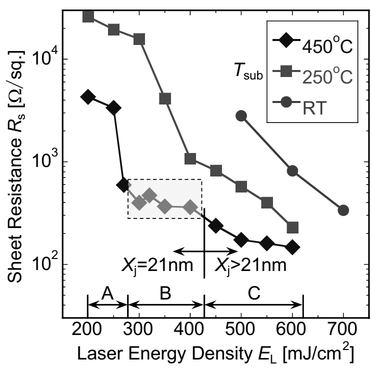
HALA & PMLA Time Sequence

Substrate Temperature (T_{sub}): **250 – 525°C**
- Laser Energy Density (E_L) : **200 – 600 mJ/cm²**
- FWHM of Laser Pulse: 38 ns, Pulse Number: 1 Pulse

Temperature Profile



Sheet Resistance and Energy Density for HALA



T_{SUB}: 450°C

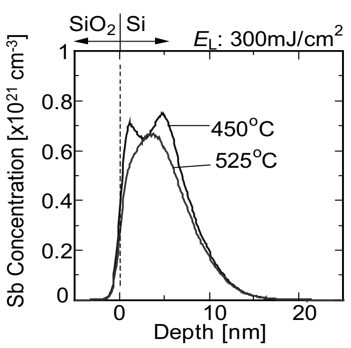
Region A
nonmelt

Region C
X_j > as Implanted
because of c-Si melt

Region B
(300-400 mJ/cm²)
Good activation
without increasing X_j

HALA: Reduction of E_L

SIMS Profile: 300 mJ/cm²



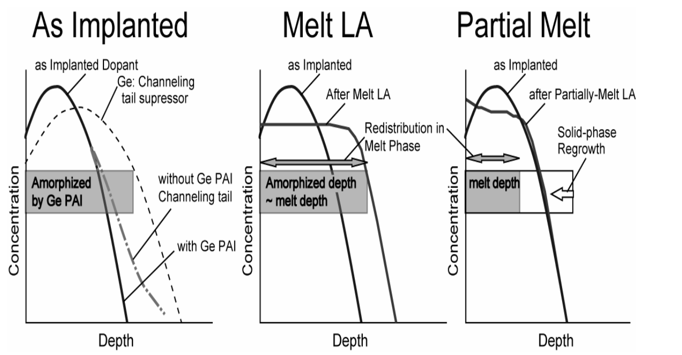
T_{sub} [°C]	Regrowth Rate [nm/min]	Regrowth Thickness [nm]
450	0.2	1
525	3	15

a-Si thickness ~ 11 nm

450°C: *Partial Melt*

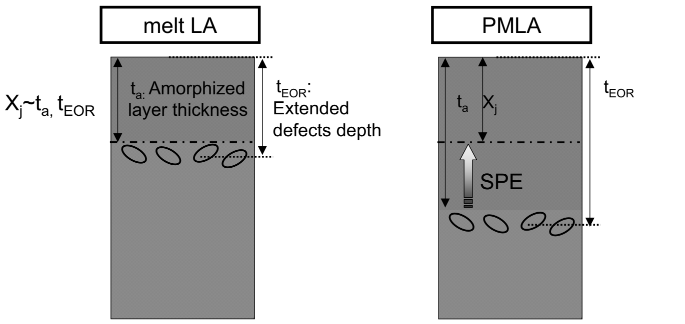
525°C: non-Melt

Basic Ideas of Schemes



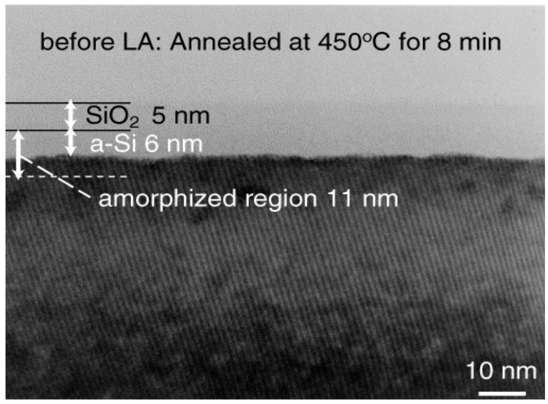
PMLA: melt(Good activation) + non-melt(Diffusion less)

Advantage of PMLA

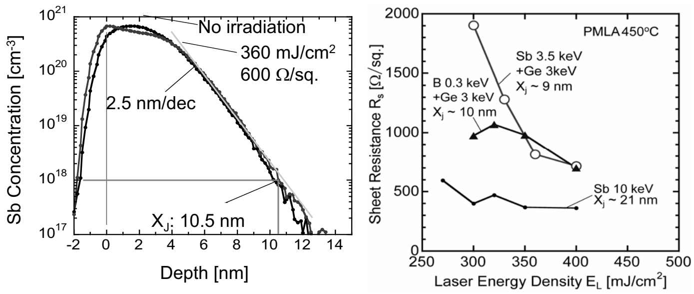


PMLA: Amorphization depth is free from junction depth

XTEM before Laser Irradiation



10 nm Junction Formation with Sb and B



Conclusions

- Achievements on metal gate and LA obtained during our COE Pj. term were reviewd.
- Metal gate and LA technologies are still exotic ones for Si LSIs. However, introduction to products is approaching.
- We will continue research to support industries by supplying better understandings on process, materials and so on related to these fields.

Acknolowdgements

This work was a result of effort of many students and researchers at RCNS and adsm of Hiroshima Univ.