A 0.6 V Supply CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization

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1. Introduction

Recently, sensor chips using mixed-signal CMOS technology have been applied for sensing and monitoring biological functions [1], [2]. A low-noise amplifier is one of the key circuits for detecting small level signals in the sensor chip. Extremely low voltage operation is required for wireless systems using such new energy sources as solar batteries or bio-batteries.

However, with increasing dc offset voltage and 1/f noise becomes a serious problem in scaled CMOS technologies. Amplifiers have large dc offset voltages caused by device mismatches. Noise reduction and calibration techniques for device mismatches are required at a low supply voltage. Autozeroing and chopper stabilization techniques are widely used for reducing these noises. However these noise reduction techniques which use floating analog switches are unsuitable for low-voltage operation [3]. The analog switches cannot transmit the intermediate voltage level at a low supply voltage, because it is not possible to scale the threshold voltage. In this paper, the design technique of an ultimately low-supply-voltage amplifier with both autozeroing and chopper stabilization techniques is presented.

2. Principle of noise reduction technique

The principle of autozeroing technique is illustrated in Fig. 1. The autozeroing technique can reduce the low-frequency noise of amplifier. Although the autozeroing technique increases baseband noise floor caused by aliasing inherent in the sampling process.The principle of chopper stabilization technique is illustrated in Fig. 2. The chopper stabilization technique converts the frequency range of input signal to a higher corner frequency, and then demodulates it back to the base band after amplification. Although the large energy is presented at a chopping frequency (fc) due to the low-frequency noise. The chopper stabilization technique equipped with a high order low pass filter (LPF) can provide the clean output signal [4], [5], [6].

Using both autozeroing and chopper stabilization techniques enable a reduction of the baseband noise floor and the modulated noise at the chopper frequency, as shown in Fig. 3. In particular at a low voltage operation, autozeroing technique is expected to resolve mismatch problem in MOSFETs.

3. Circuit architecture and Low-voltage design

3.1 Circuit architecture

Figure 4 shows a circuit of the low-noise amplifier with autozeroing and chopper stabilization technique operating at a low supply voltage. The chopper modulators (Chopper1, 2) placed in the virtual ground are implemented by simple analog switches, because a voltage level of virtual ground is possible to set to any level and signal voltage swing is small. The demodulator Chopper3 has large signal voltage swing. Therefore the Chopper3 is implemented by the multi-output SWOPA (switched op-amp). The multi-output SWOPA can configure the autozeroing scheme. During the phase Φ0, the output of multi-output SWOPA are connected to its input using dotted lines as shown in Fig. 4, so that it forms a voltage follower. The detected dc offset voltage is sampled into the hold capacitor C3, accordingly, the autozeroing operation cancels the dc offset.

3.2 Multi-output switched op-amp (SWOPA)

Figure 5 shows the circuit schematic of multi-output SWOPA. The multi-output SWOPA consists of 3stages. The input stage is implemented with a PMOS differential pair. The second stage consists of common-source gain stages and bias stages, and they drive final buffer stages operating class AB. The final stage consists of the demodulator Chopper3 and the autozeroing outputs. The output buffers are switched by the complementary clock Φ0, Φ1 and Φ2.

The input stage of multi-output SWOP limits decreasing of supply voltage. The multi-output SWOP doesn't need a wide input voltage range, because it's input is virtual ground. Input common mode voltage is set to 0V, and voltage of node G is decided to 0.55V by setting over drive voltage 0.05V. As shown in eq. (1) the supply voltage can be decreased to 0.6V (Vthp= -0.5 V).

$$V_{in} + V_{gs}(M2, 3) + V_{ds}(M1) = 0.6V \quad (1)$$

The input voltage range needs to set near 0V. The output stage operates in class AB. Voltage range is

$$V_{ss}+0.05(V) < \text{Output voltage range} < V_{dd}-0.05(V) \quad (2)$$

3.3 Common-mode feedback circuit (CMFB)

Figure 6 shows the circuit schematic of the Common-mode feedback circuit (CMFB). The output common-mode level of the SWOPA is detected using a resistive divider and compared with the reference voltage of 300 mV. It is returned to the feedback nodes of the comn and comp in fig. 5. The MOSFETs of the CMFB circuit are operated in the threshold region. The low-noise amplifier has two CMFB circuits. CMFB1 operates in phase 0 and CMFB2 operates in phases 1 and 2 in fig. 4. The CMFB circuits are switched with rst and rst_ in phase 0 or phases 1 and 2.

3.4 Monte Carlo analysis

Device deviation causes a large dc offset voltage at a low supply voltage. In particular, the mismatches of the input parts (M2, M3, M4, M5 in Fig .5) are a serious problems. The influence of the mismatch and the effect of the autozeroing technique were confirmed by Monte Carlo analysis. The mismatches of Vth, L, and W were considered. Device deviation parameters provided by a fabricating lab were used. Figure 7 shows the simulation result of a Monte Carlo analysis. As shown in Fig. 7(a), large dc offset voltages cause the output of the amplifier to become saturated without autozeroing. On the other hand, the autozeroing technique suppresses the output offset voltage to $\pm$9.6 mV, as shown in Fig. 7(b). The simulation result shows that the autozeroing technique can calibrate device mismatches and decrease the dc offset voltage.

4. Experimental results

A test chip for a low-noise amplifier with chopper stabilization and autozeroing techniques was fabricated by a 0.18 μm CMOS process (Vthn = 0.42 V, Vthp = -0.5 V). The micrograph of the test chip is shown in Fig. 8. The chip area is 0.49×0.38 mm^2.

The measurement results are shown in Figs. 9, Figs 10 and Figs. 11. The low-noise amplifier was operated with a 1 MHz chopping frequency and a 5 μs autozeroing time at a supply voltage of 0.6 V. The output waves of the amplifier are shown in Figs. 9. The output offset voltage of the multi-output SWOPA was 270 mV. The autozeroing technique suppresses the output offset voltage to 3.3 mV. That result clearly shows that the autozeroing technique can resolve mismatch problem of MOSFETs at a low voltage operation. The input noise PSD of the amplifier is shown in Figs. 10. The input noise without chopper and autozeroing shows a typical 1/f noise spectrum. When chopper and autozeroing suppress the input noise, the noise PSD is 89 nV/√Hz at 1 kHz.

The frequency response of the voltage gain is shown in Fig. 11 (a). The amplifier achieved a 32 dB voltage gain and a 1.6 MHz cut-off frequency. The unity gain frequency was 10 MHz. The frequency responses of CMRR, PSRR+ and PSRR- are shown in Fig 11 (b). The CMRR, PSRR+ and PSRR- were 52 dB, 64 dB and 72 dB at 1 kHz, respectively. A comparison between the performance of reference amplifiers and the proposed amplifier is shown in Table I. When defining the figure of merit (FOM), we focused on input noise, power consumption, and chip area; the equation is as follows:

$$\text{Figure of Merit (FOM)} = 1000/(\text{Input noise} \times \text{Power consumption} \times \text{Chip area}) \quad (3)$$

We proved that an amplifier using the autozeroing and chopper stabilization techniques can operate with a 0.6 V power supply. The FOM of the proposed amplifier achieved a result 10.2 times larger than the referred amplifiers [3], [4], [5].

5. Conclusions

The noise reduction technique and the calibration technique of mismatch at a low supply voltage have been presented. The proposed techniques achieve autozeroing and chopper stabilization techniques without analog switches. The key points of these techniques are multi-output switched op-amp, chopper modulator implementation in the virtual ground, and the use of a capacitor for storing up dc offset voltage. A low-noise amplifier with autozeroing and chopper stabilization techniques was fabricated with a normal Vth 0.18 um CMOS process has achieved 89 nV/√Hz noise PSD, 10 MHz unity gain bandwidth and 0.13 mW power consumption when utilizing a 0.6 V supply voltage.

Acknowledgements

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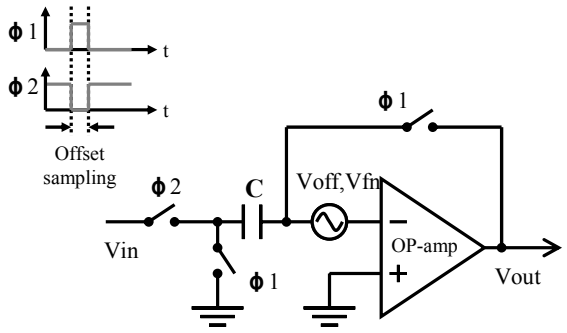


Fig.1 Principle of Autozeroing technique.

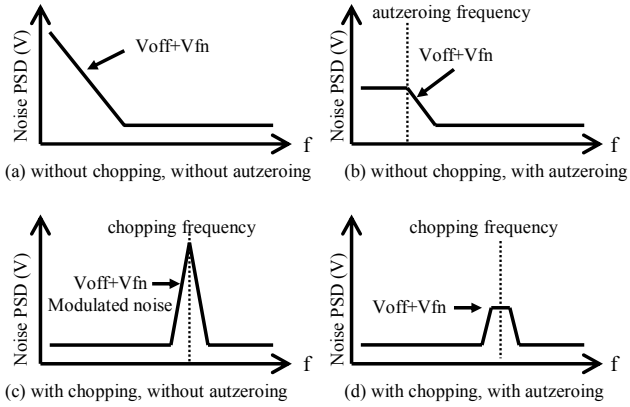


Fig. 3 PSD with/without noise reduction technique

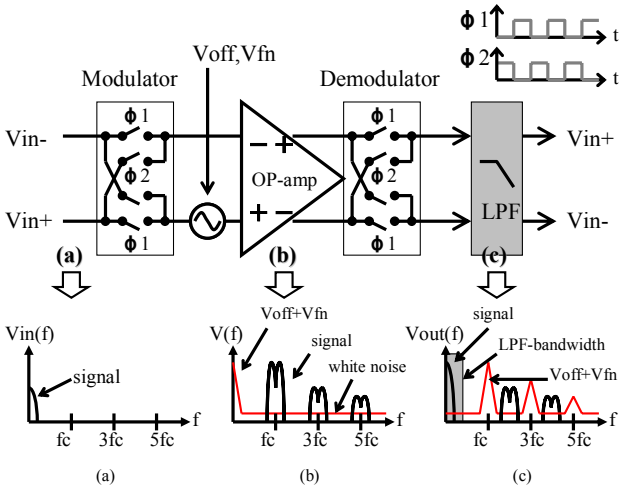


Fig. 2 Principle of Chopper Stabilization technique.

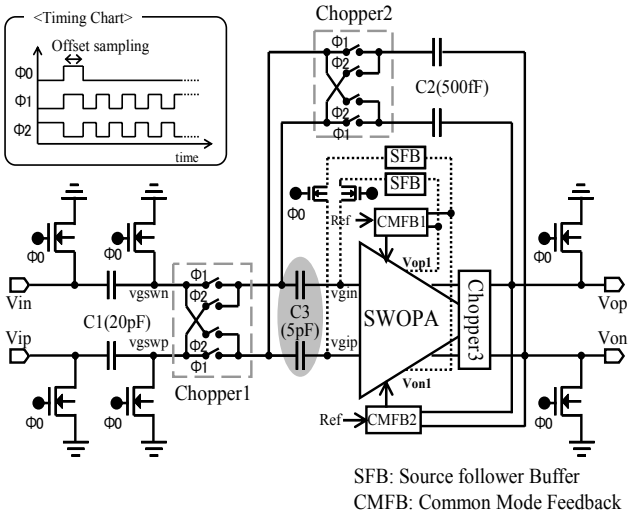


Fig. 4 A circuit of low-noise amplifier

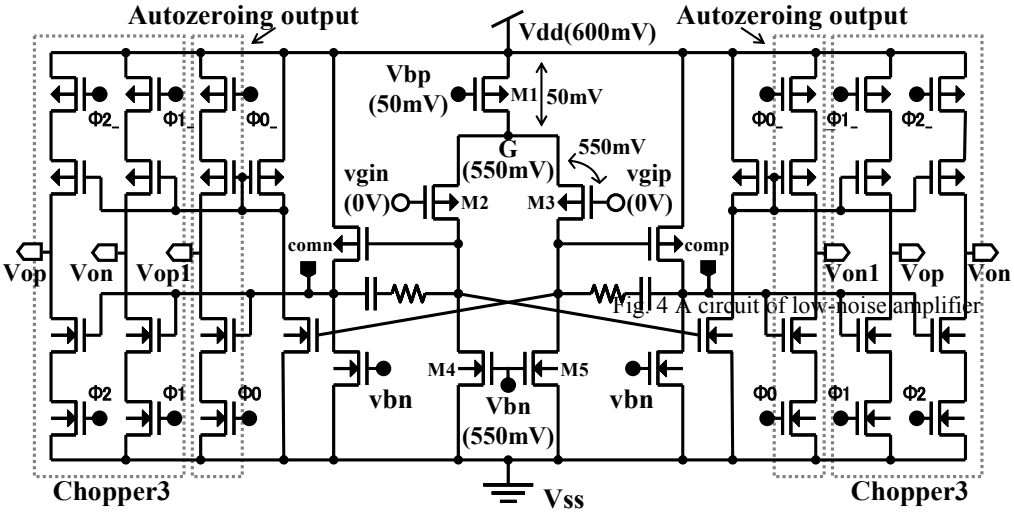


Fig. 5 Schematic of the fully-differential multi-output SWOPA.

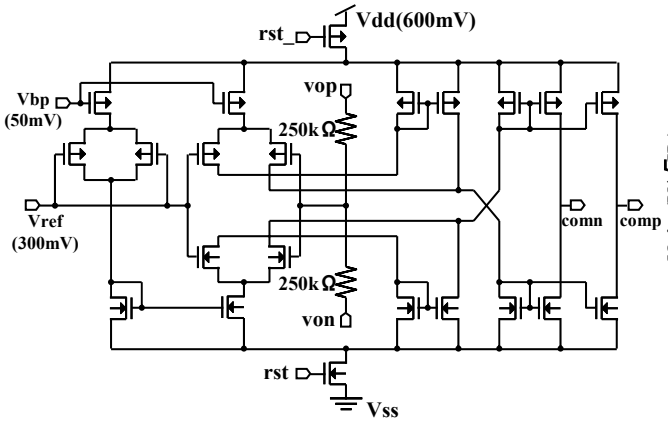
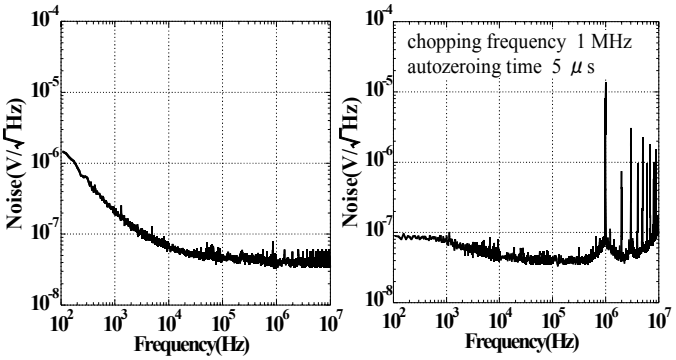


Fig.6 Schematic of CMFB.



(a)Without chopper and autozero (b)With chopper and autozero

Fig. 10 Input noise PSD.

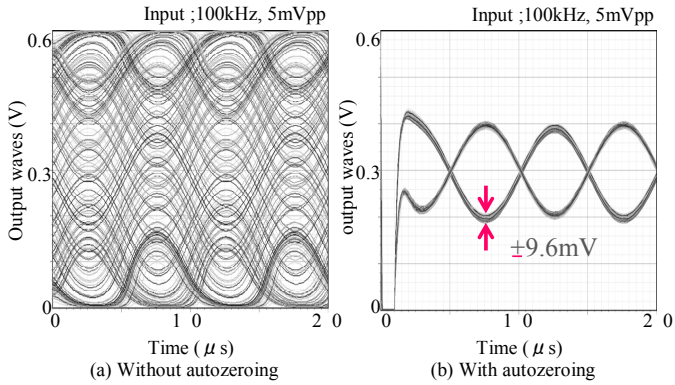
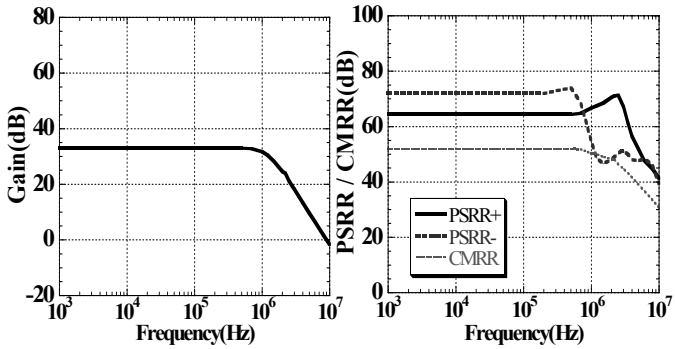


Fig.7 Simulation result of Monte Carlo analysis.



(a) Frequency response (b) PSRR / CMRR

Fig. 11 Frequency response.

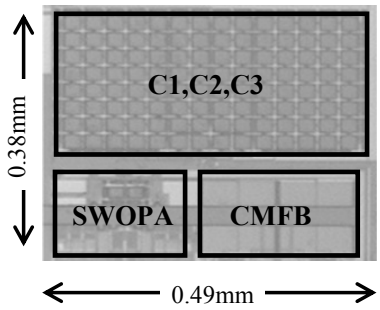
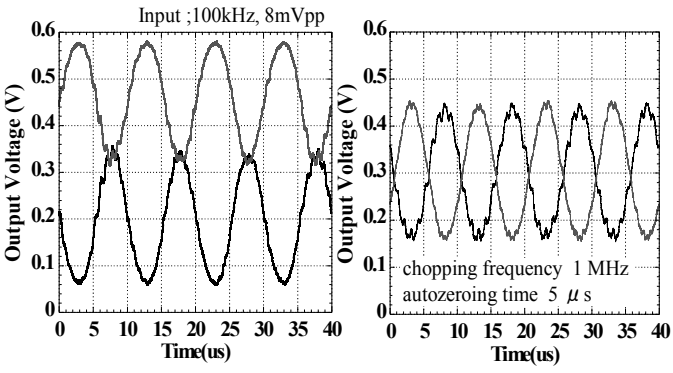


Fig.8 Chip micrograph.



(a)Without chopper and autozero (b)With chopper and autozero

Fig. 9 Output waves.

Table I Comparison of the reference op-amps and this work.

	This study	Ref, 3	Ref, 4	Ref, 5
Year of publication	2006	2005	2002	2000
Supply voltage (V)	0.6	1.0	5.0	1.0
Autozeroing frequency (kHz)	<0.001	<0.001	7.5	-
Chopping frequency (kHz)	1000	1000	15	-
Input noise PSD at 1kHz (nV/√Hz)	89	50	20	360
Power consumption (mW)	0.13	0.5	4.0	0.2
Chip area (mm^2)	0.186	0.88	0.67	0.81
Unity gain bandwidth (MHz)	10.0	20.2	2.5	2.1
FOMx10^3	464.7	45.5	18.7	17.1