HiSIM-SOI: Complete Surface-Potential-Based Fully-Depleted SOI-MOSFET Model for Circuit Simulation

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Abstract

The circuit simulation model for fully-depleted SOI-MOSFET is developed based on the surface-potential description considering the potential distribution vertical to the channel and parallel to the surface explicitly. Besides the comparison to measured *I-V* data, the model is verified with 1/*f* noise analysis, sensitive to the carrier concentration and distribution along the channel. And furthermore, for the accurate modeling of the short channel effects, the parasitic electric field induced through the buried oxide is considered

1. Introduction

Various types of MOSFETs, such as SOI-MOSFET and double-gate MOSFET, have been developed for further integration and improvement of circuit performance [1]. The compact models for circuit applications are now under development with different approaches [2]. Our objective is to develop a circuit simulation model for the fully-depleted SOI-MOSFET as the first step for describing phenomena caused by the channel confinement between two oxide layers. Advantage of pursuing the fully-depleted SOI-MOSFET is that the modeling accuracy is easily verified by measured characteristics of production-level SOI-MOSFET technologies.

Existing SOI-MOSFET models are suffering convergence problems in circuit simulation, due to the violation of the charge conservation. As shown in Fig. 1, in SOI-MOSFETs, there are three Si-SiO_2 interfaces to induce charges. Thus surface-potential-based modeling is the only solution for the SOI-MOSFET to secure the charge conservation in a consistent way. We have developed the SOI-MOSFET model HiSIM-SOI based on this charge conservation guideline. Our investigation here focuses on carrier density changes in the SOI channel in comparison to the bulk-MOSFET. Because the 1/*f* noise characteristics are sensitive to the carrier concentration as well as its density distribution in the channel, we have studied the 1/*f* noise characteristics. The short channel effects are of serious concern for scaled devices, and to model these effects accurately is indispensable for reliable circuit simulation. To include short channel effect of SOI-MOSFET accurately, we considered not only the electric field lateral to the channel, which is already modeled in HiSIM for bulk MOSFET, but also the electric field comes via buried oxide.

2. Method and Results

To include all device features of the SOI-MOSFET accurately, HiSIM-SOI determines not only the surface-potential at the channel surface, but also at the back side, as well as at the bulk back-gate self-consistently as schematically depicted in Fig. 1 [4]. The total iterative potential calculation requires only about twice as much calculation time as for the bulk-MOSFET case, solving just at the channel-surface. Fig. 2 demonstrates the accuracy of the three calculated surface potentials in comparison to the results with the 2D-device simulator. Fig. 3 compares HiSIM-SOI simulation results of the channel-inversion charge with a 2D-Device Simulator for two silicon-layer thicknesses T_{SOI}. The model reproduces measured *I-V* characteristics within numerical accuracy as shown in Fig. 4, and is verified to show stable convergence in circuit simulation.

Fig. 5 compares simulation result of the 1/*f* noise with measurements. Deviation of three measurement points (open triangles) from simulation results is attributed to impact ionization, called as low frequency excess noise [5][6].

Fig. 6 shows electric field distribution in the SOI channel region calculated by 2D-Device simulator. This parasitic electric field is considered as one of the cause of short channel effect in SOI-MOSFET, and we modeled this effect analytically in HiSIM-SOI. Fig. 7 shows V_{th}-L_{gate} characteristics of HiSIM-SOI in comparison with 2D-Device simulation result. HiSIM-SOI calculation with parasitic electric filed model show good agreement with 2D-Device simulation result.

3. Conclusion

A circuit simulation model for the fully depleted SOI-MOSFET has been developed based on a complete surface-potential description. In addition to the conventional short channel effect due to horizontal electric field in the channel, the effect of the field from the source/drain contacts through the buried oxide must is included in the compact model to reproduce V_{th}-L_{gate} characteristics. The developed surface-potential based model for the SOI-MOSFET is verified to reproduce measured *I-V* characteristics as well as 1/*f* noise data. The model is named HiSIM-SOI and implemented into the circuit simulator SPICE 3F5.

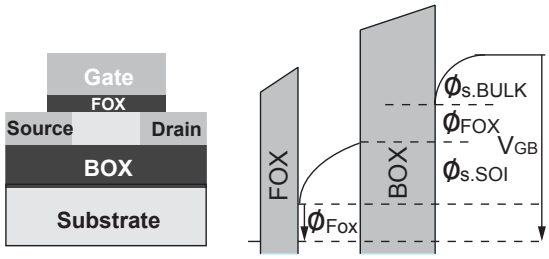

Fig. 1. Schematics of the fully-depleted SOI-MOSFET. The three surface potentials are solved iteratively with the Poisson equation.

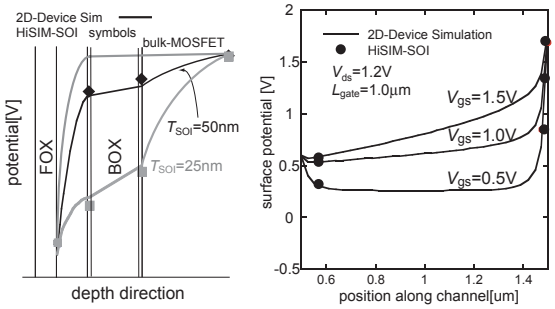

Fig. 2. Comparison of HiSIM-SOI calculated surface potentials with the results of a 2D-device simulator.

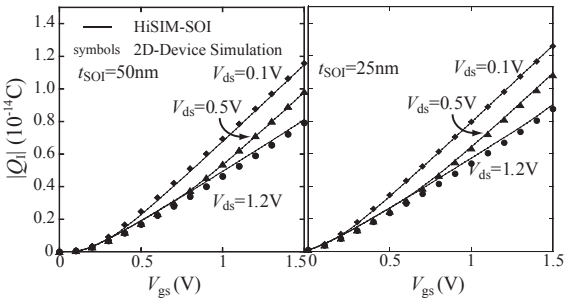

Fig. 3. Comparison of calculated inversion charge Q_I with a 2D-Device Simulation results, for a silicon-layer thickness of (a) 50nm and (b) 25nm.

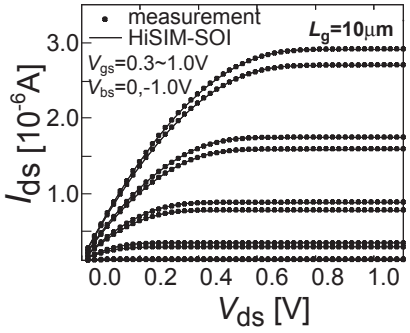

Fig. 4. Calculated drain current I_{ds} as a function of drain voltage V_{ds}. Symbols are measurements.

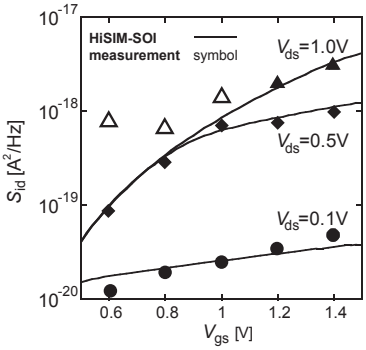

Fig. 5. Calculated 1/*f* noise density as a function of gate voltage V_{gs} at f=100Hz. Symbols are measurements. Deviation of the three open triangles from the HiSIM-SOI result is attributed to impact ionization.

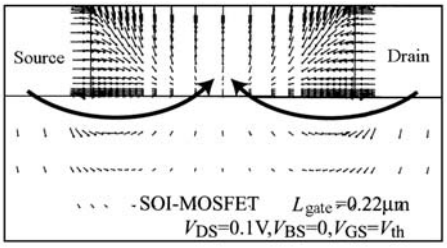

Fig. 6. Electric field distribution in the channel region of SOI-MOSFET simulated by 2D-Device simulator.

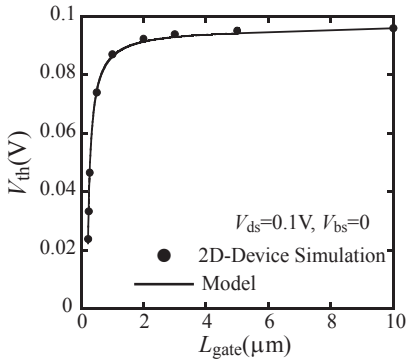

Fig. 7. V_{th}-L_{gate} characteristics of SOI-MOSFET of HiSIM-SOI shown by line in comparison with 2D-Device simulation result.

References

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