Multi-Bank Register File for Increased Performance of Highly-Parallel Processors

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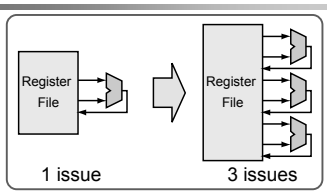
Backgrounds

Processor trends

Execution of multiple instructions in the same clock cycle.
Superscalar processor
VLIW processor
Much higher parallelism

Increase of port number and storage capacity



Increase of port number due to multiple instruction execution.

As the number of ports increases,
- Area penalty due to port-related routings
- Increasing access delay time
- Increasing power dissipation

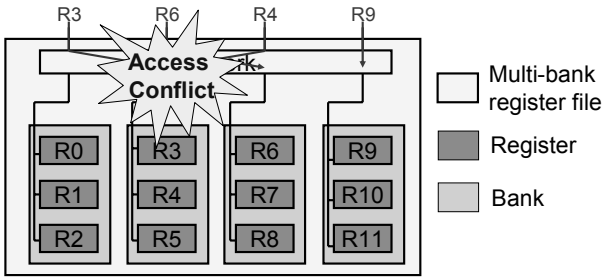
Register file becomes the performance bottle neck for highly parallel processors.

It is necessary to find a more suitable multi-port register file architecture for highly parallel processors.

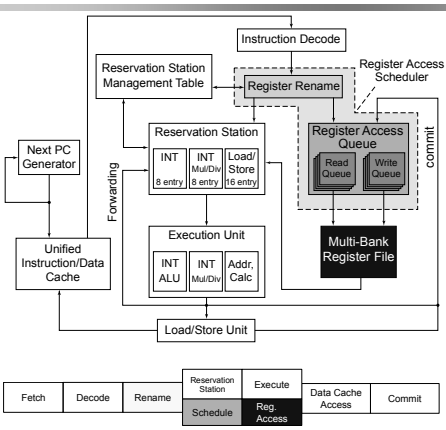
Proposal of multi-bank register file

Access Conflict Problem

- Using multi-bank register file, causes an access conflict problem.
- Access conflicts decrease the clock-cycle-based performance of the processor.



Processor Architecture with Multi-Bank Register File

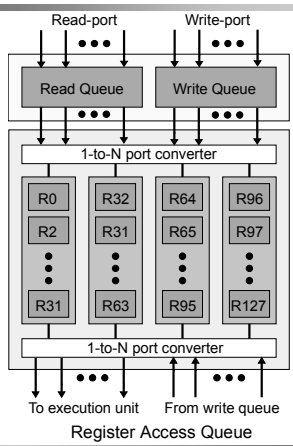


Execution pipeline of processor

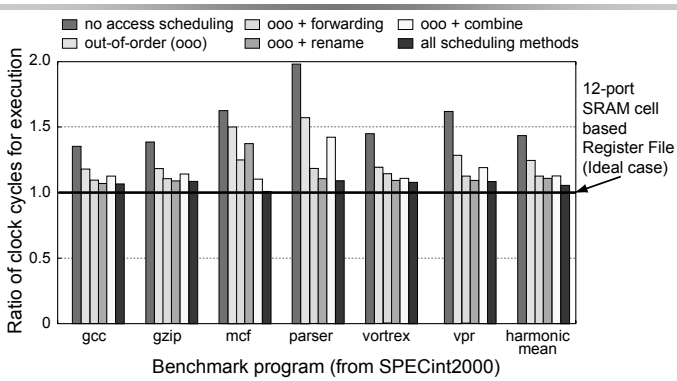
- MIPS10000 instruction set
- 4 instruction fetches
- 7 pipeline stages
- Multi-bank register file
  4 banks,
  8-read & 4-write ports,
  128 entries,
  32 bit word length
- Register access scheduler for out-of-order register access
- Unified data/instruction cache with distributed crossbar.

Access Scheduling Method for Reduced Conflicts

- Register renaming
  - Register renaming with consideration of the bank structure
- Reduction of the number of register accesses
  - Combining accesses to the same register as much as possible
  - Forwarding of previous results to execution units
- Register access queues for out-of-order register access
  - Access conflicts to a bank are avoided by storing the data of conflicting register-file accesses temporarily.



Evaluation of Register Access Scheduling Efficiency

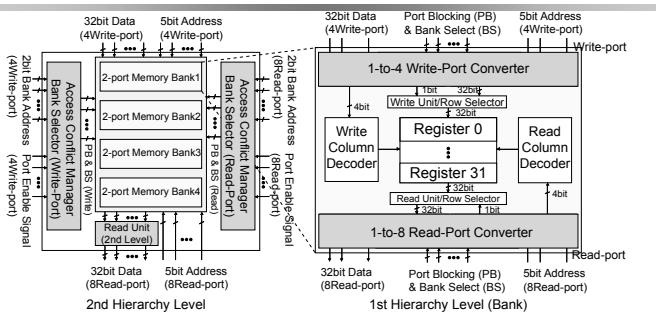


Proposed method increases clock cycle number only by 5% in average.

Important Features of the Designed Test Chip

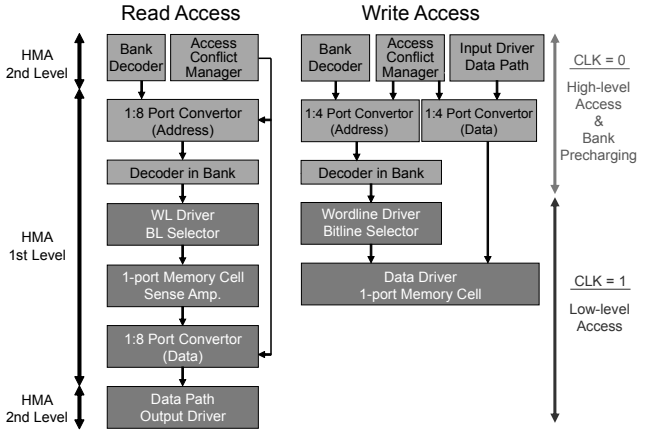
- Multi-bank register file based on distributed crossbar architecture (Hierarchical Multi-port memory Architecture : HMA)
- 2-port SRAM cells and port converters (1-to-8 read- and 1-to-4 write-port converters) are integrated in each bank.
  - 2-port SRAM cell has 1-read and 1-write port.
  - Area is reduced due to reduction of port-related signal lines.
- Access method with hidden pre-charge
  - Minimization of the access time
- Effective floorplan with HMA
  - Decoder and controller are placed at the center of each bank.
  - Global signal lines are designed without bending.

Architecture of 12-port multi-bank HMA register file

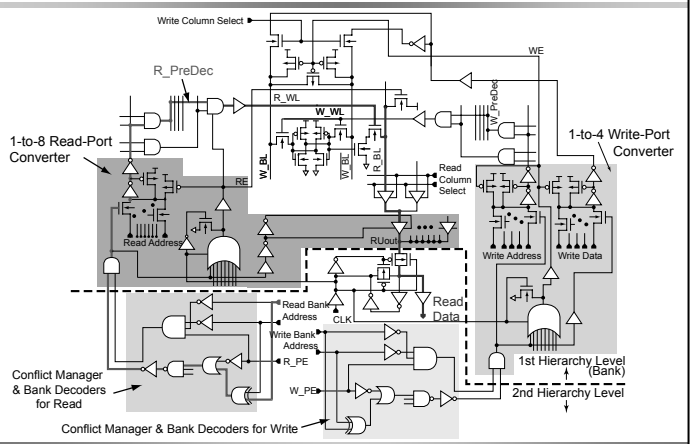


- 2 port SRAM cells and 1-to-8 read-port, 1-to-4 write-port converters are used in each bank.
  - Reduction of area and access delay time.
- Access conflicts are avoided by,
  - Access scheduler integrated after instruction decoding in the processor.
  - Completely divided read and write path until SRAM cells.

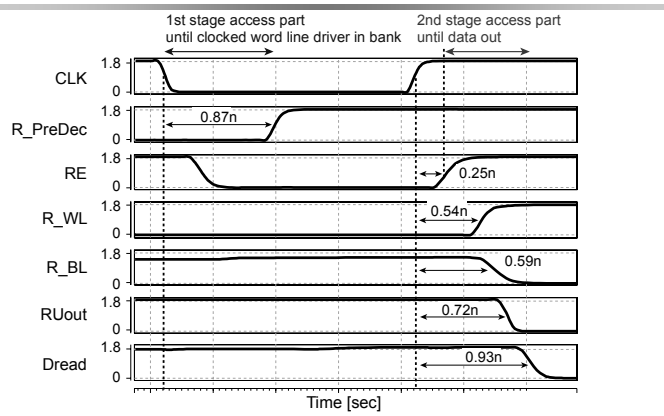
Hidden Precharge Method



Critical path of the Test Chip

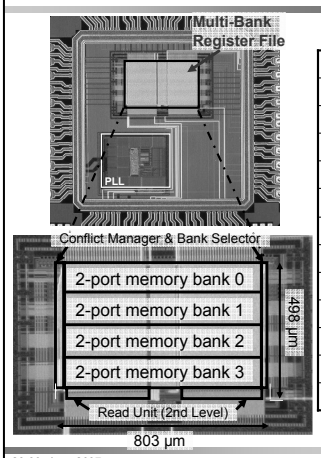


Timing Diagram with Simulation Results



Minimum CLK cycle : 0.87 + 0.93 - 0.25 = 1.55 nsec

Test Chip Photomicrograph and Design Data

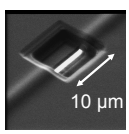


Specification of test chip

Technology	Std. CMOS w/o SRAM rules
Min. gate length	200 nm
# of metal layers	5 Al routing layers
Supply voltage	1.8 V
Die area	2.8 mm × 2.8 mm
Port number	8 read & 4 write ports
# of registers	128 entries
Total capacity	4 Kbit
Bank capacity	1 Kbit
Bank number	4 bank
Word length	32 bit
Max. frequency	640 MHz (simulated)
Core area	498 µm × 803 µm

Measurement Results

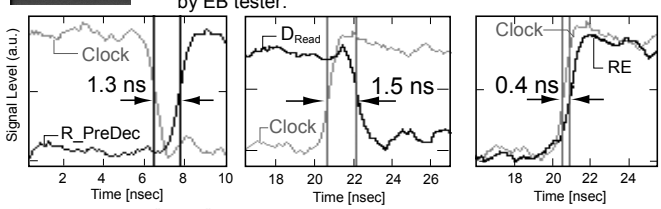
With a conventional logic analyzer environment,
the test chip function could be tested only up to 200 MHz.



For higher frequencies an electron beam (EB) tester was used.

→ Film removal above measurement points with Focused Ion Beam (FIB) facility.

→ Signal measurement within the chip directly by EB tester.

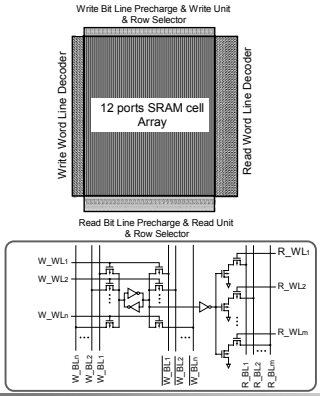


CLK transition "0" to "1" can occur 0.4 ns before R_PreDec rises.

→ Minimum CLK cycle : 1.3 + 1.5 - 0.4 = 2.4 nsec

Comparison with Conventional Register Files 1

A. Conventional 12-port register file design in the same spec & technology (200 nm CMOS)

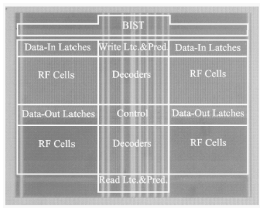


	Multi-bank Register File (HMA)	Conventional Multi-port-cell Register File
Technology	200nm L_{gate} 5 metal CMOS	200nm L_{gate} 5 metal CMOS
Supply voltage	1.8 V	1.8 V
Access ports	12 (8r, 4w)	12 (8r, 4w)
Registers	128	128
Word length	32 bit	32 bit
Core area	0.39 mm^2	1.43 mm^2
Max operation frequency	640 MHz (simulated) 417 MHz (measured)	330 MHz (simulated)
Power dissipation	210 mW @500 MHz (simulated)	105 mW @330MHz (simulated)

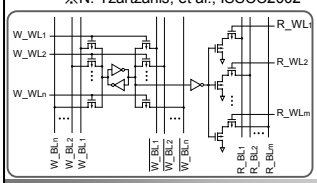
95 % higher clock frequency
73 % smaller area

Comparison with Conventional Register Files 2

B. Conventional high-performance register file with different spec & technology (110nm CMOS)



※N. Tzartzanis, et al., ISSCC2002



	Multi-bank Register File (HMA)	Multi-bank Register File (HMA), **estimated**	Conventional Multi-port-cell Register File ISSCC2002
Technology	200nm L_{gate} 5 metal CMOS	110nm L_{gate} 5 metal CMOS	110nm L_{gate} 4 metal CMOS
Supply voltage	1.8 V	1.2 V	1.2 V
Access ports	12 (8r, 4w)	16 (10r, 6w)	16 (10r, 6w)
Registers	128	34	34
Word length	32 bit	64 bit	64 bit
Core area	0.39 mm^2	0.21 mm^2	0.5 mm^2
Max operation frequency	640 MHz (simulated) 417 MHz (measured)	1140 MHz (from sim.) 746 MHz (from meas.)	545 MHz (measured)
Power dissipation	210 mW @500 MHz (simulated)	106 mW @500 MHz (from sim.)	220 mW @500 MHz

37 % higher clock frequency
58 % smaller area
52 % lower power dissipation

Conclusions

- Multi-bank register file is proposed for highly parallel processors and verified with a test chip.
  - Cycle-based performance reduction due to conflict problems is only 5% with the proposed scheduler.
  - 12-port register file clock frequency has been evaluated by a design, fabrication and simulation study with 200nm CMOS technology.
    Max. freq : 640 MHz (from sim.) , 417 MHz (from meas.)
- Comparison with conventional multi-port cell register files
  - 12-port cell register file under same spec & technology
    95 % clock frequency improvement, 73 % area reduction
  - Conventional high-performance register file with different spec & technology
    37 % clock frequency, 58 % area, and 52 % power dissipation improvement
  - Up to a factor 2 higher overall instruction execution performance can be expected for the processor.