On-Chip Wireless Signal Transmission using Silicon Integrated Antennas

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1. Introduction

In order to realizing three-dimensional (3D) multiple packaging of ultra large scale integrated circuits (ULSI), wireless interconnect has been proposed, which utilizes electromagnetic (EM) wave by using on-chip antenna integrated in LSI chips.[1-4] Figure 1 illustrates a conceptual diagram of intra-/inter-chip wireless interconnect using Si integrated dipole antennas in multiple stacked Si ULSI chips. Transmitting antennas on a chip having a function distribute clock signals and transmit data signals for receiving antennas on another chip having a different function by operating EM wave propagation for intra-/inter-chip. As a communication system in ULSI chips, we use impulse radio based ultra wideband (UWB) communication, because of higher-speed signal transmission and low power consumption. According to Shannon's theorem as described eq. (1),

$$C = B \log_2\left(1+\frac{S}{N}\right) \tag{1}$$

data rate (C) between LSI chips can be increased by increasing bandwidth (B) of wireless interconnect channel. UWB technology is necessary for intra-/inter-chip higher-data transmission. As one of issues for realizing wireless interconnect of LSI using Si integrated antennas, its frequency and time domain characteristics must be analyzed.

Another issue of UWB communication is the interference from other communication system, especially wireless local area network (WLAN). Therefore, we investigated the influence of WLAN at 5.2 GHz in UWB communication, and then we designed an integrated notch filter using 0.18-μm CMOS technology to suppress the influence of WLAN.

In this paper, we demonstrated a feasibility of wireless interconnect using on-chip integrated dipole antennas in stacked ULSI chips. First, we investigated transmission characteristics of integrated dipole antennas in stacked Si chips.[5] Then, we designed the notch filter integrated on Si chips to suppress the influence of WLAN at 5.2 GHz.[6] Finally, the equivalent circuit model of Si integrated dipole antenna including propagation channel was developed for analyzing the transmission characteristics.[7]

2. Experimental

Fabrication process is a conventional LSI process technology. P-type (100) Si wafers were prepared as substrates which thickness of 260 μm and resistivity of 10 Ω·cm. The Si surface was oxidized to form 0.3-μm thick field SiO_2. A 1.0-μm thick aluminum layer was deposited on the SiO_2 layer by direct current (DC) magnetron sputtering, and then integrated dipole antenna patterns were formed using HL-700 electron-beam (EB) lithography.

Figure 2 shows the integrated dipole antennas for transmitting and receiving signals. A typical antenna length (L) is 4 mm in this paper. Sample wafers were measured on a low-k substrate (wood) with 2.6-mm thick on the metal chuck of the probe station in order to eliminate the capacitance coupling between antennas and metal chuck.[8] The relative dielectric constant of wood is 2.15 at 1 GHz.

A wafer level measurement set-up for scattering parameter (S-parameter) in the frequency domain is shown in Fig. 3. It consists of HP8510C vector network analyzer, 180° hybrid couplers (KRYTAR; 6-26.5 GHz), probe station and signal-signal (SS) probes. From measured S-parameters, reflection coefficient (S_{11}) and transmission coefficient (S_{21}), transmission characteristics were investigated in the frequency domain. Figure 4 shows a measurement set-up for UWB signal transmission. It is composed of Agilent N4902B serial bit error rate tester (BERT), two impulse forming networks (IFNs, Picosecond), and Agilent 86100C sampling oscilloscope.

3. Results and Discussion

3. 1. Transmission characteristics of integrated dipole antennas in stacked Si chips

Figure 5 shows a sample structure for the measurement of EM wave transmission characteristics through stacked Si chips using integrated dipole antennas. Number of the inserted Si chips between transmitting and receiving antennas (N) was changed from 0 to 10. Thickness of Si chip is 0.26 mm per a chip, so that line-of-sight (LOS) distance between transceiver antennas changed from 3.01 to 4.14 mm. Figure 6 shows the influence of the number of inserted Si chips on reflection coefficient (S_{11}) when changing frequency from 6 to 26.5 GHz. Resonance frequency at 14 GHz for N=0 changed slightly lower frequency with increasing the number of inserted Si chips, because effective dielectric constant (ε_{eff}) increased with increasing the number of inserted Si chips as described eq.(2),

$$f_{res} = \frac{f}{\sqrt{\varepsilon_{eff}}} \tag{2}$$

where f_{res} is resonance frequency on Si chip and f is resonance frequency in air. Figure 7 shows the influence of the number of inserted Si chips on transmission coefficient (S_{21}). S_{21} decreased with increasing the number of inserted Si chips because of increasing lossy propagation channel in stacked Si chips.

Next, time domain characteristics were investigated. Figures 8(a) and 8(b) show transmitting Gaussian

monocycle pulse and its frequency spectrum. Its pulse width is 70 psec, center frequency is 15 GHz, and band width is 20 GHz. Received Gaussian monocycle pulse for N=10 was shown in Fig. 9. Its peak-to-peak voltage was 0.4 mV. The received signal was distorted due to band-pass characteristics of the transceiver antennas. Figures 10(a) and 10(b) show dependence of the number of inserted Si chips on transmission gain at the frequency of 20 GHz and received peak-to-peak voltage of Gaussian monocycle pulse. Propagation loss decreased from –1.3 dB/chip to –0.14 dB/chip by increasing the resistiviety of inserted Si chips from 10 to 2290 $\Omega \cdot$cm for 20 GHz sinusoidal wave propagation. Propagation loss of received peak-to-peak voltage also improved from –0.08 mV/chip to –0.03 mV/chip by inserting high resistivity Si chips.

3. 2. Integrated notch filter

To eliminate the frequency band of WLAN around 5.2 GHz from received UWB signals, we designed the integrated notch filter. A chip photograph of designed notch filter fabricated by use of 0.18-μm CMOS technology is shown in Fig. 11 and its equivalent circuit is shown in Fig. 12. Its chip area was 860×600 μm^2. The parameters of LC elements were L=4.9 nH, C=159 fF, L'=1.68 nH, C'=517 fF, L''=0.7 nH, and C''=517 fF, respectively. Two parallel L and C networks resonate and make a notch at 5.2 GHz. In additional, a shunt series L' and C' resonance network enhances the notch. L'' and C'' work for an impedance matching between the receiving antenna and the notch filter. Figures 13(a) and 13(b) show measured and simulated reflection coefficient (S_{11}) and transmission coefficient (S_{21}), respectively. Measurement data showed good corresponding to the simulation results. It was found that a notch was observed at 5.2 GHz and separation was approximately –40 dB.

Figure 14 shows measurement for the influence of interference to the UWB communication. A left hand linear dipole antenna transmits pseudo random Gaussian monocycle pulse trains as UWB signals, a center meander dipole antenna transmits 5.2 GHz sinusoidal wave as the interference signal, and a right hand linear dipole antenna receives these signal. Figure 15 shows received UWB signals by linear dipole antenna with the interference signal of 5.2 GHz sinusoidal wave radiated from the meander dipole antenna. Peak-to-peak voltage of received signal is 3.8 V. UWB pulse trains could not be observed at all. On the other hand, through the integrated notch filter, the interference signal was eliminated from received signal by HSPICE simulation as shown in Fig. 16. As a result, UWB pulse trains were observed successfully with peak-to-peak voltage of 0.48 V.

Figure 17 shows bit error rate (BER) versus received signal to interference signal ratio when Gaussian monocycle pulse trains of 32,767 bit pseudo random binary sequence (PRBS) was transmitted with and without the notch filter. By use of the integrated notch filter, interference was suppressed, so that BER was improved. BER was below 3.05×10^{-5}, when received signal to interference signal ratio was over –6.05 dB.

3. 3. Equivalent circuit model of Si integrated antennas

We developed an equivalent circuit model of Si on-chip dipole antenna including transmission medium for CMOS integrated circuits to analyze the UWB transmission characteristics in ULSI chips. Figure 18 shows the proposed equivalent circuit model. Transmitting and receiving antennas consisted of RLC (R_{rad}, C_{ant}, and L_{ant}) series resonant circuits and they were fabricated on Si chips, so that parasitic components (C_{SiO2}, R_{Si}, C_{Si}, and C_{low-k}) were added. Signal propagation channel was modeled as a transmission line (R, L, R_{sub}, and C_{sub}). Parameters fitting of equivalent circuit model were carried out using Agilent advanced design system (ADS). Figure 20(a) and 20(b) show comparison the simulation of equivalent circuit model with the measurement on S_{11} and S_{21} for transmission characteristics of stacked Si chips, respectively. The simulation results using the equivalent circuit model fitted well with the measurement data of S_{11} and S_{21}. Using extracted RLC parameters, received waveform of Gaussian monocycle pulse was simulated by HSPICE circuit simulator in time domain as shown in Fig. 20. The simulation result could reproduce the measurement data.

4. Conclusion

A feasibility of wireless signal transmission through stacked Si chips using on-chip integrated antennas was demonstrated. Gaussian monocycle pulse was transmitted successfully through stacked Si chips and received peak-to-peak voltage was 0.4 mV. The propagation loss was improved by inserting high resistivity Si chip. Influence of WLAN at 5.2 GHz on UWB data transmission between Si chips were investigated and suppressed by use of the integrated notch filter fabricated on Si chip. Equivalent circuit model was developed for Si on-chip integrated antennas and RLC parameters were extracted. Using the equivalent circuit model and extracted RLC parameters, received signal waveform of Gaussian monocycle pulse through stacked Si chips could be reproduced by HSPICE circuit simulator successfully.

References
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[8] S. Watanabe et al, Jpn. J. Appl. Phys., Vol. 43, No. 4B, 2004, pp.2297-2301.
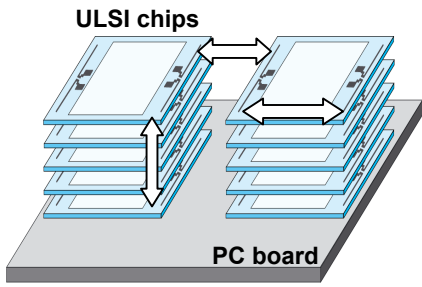
Fig. 1. Concept diagram of intra-/inter-chip wireless interconnect using dipole antennas integrated in multiple stacked Si ULSI chips.
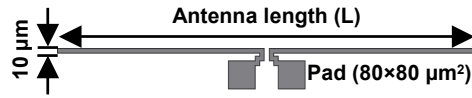

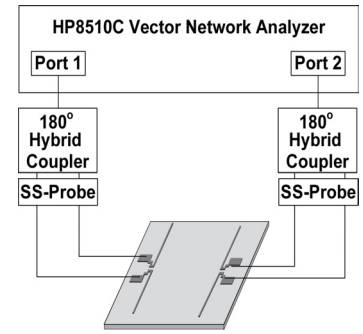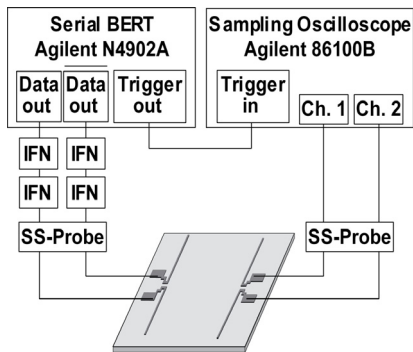Fig. 2. Si integrated linear dipole antenna used for transmitting and receiving signal.

Fig. 3. Measurement set-up for antenna transmission characteristics in frequency domain.

IFN : Impulse Forming Network

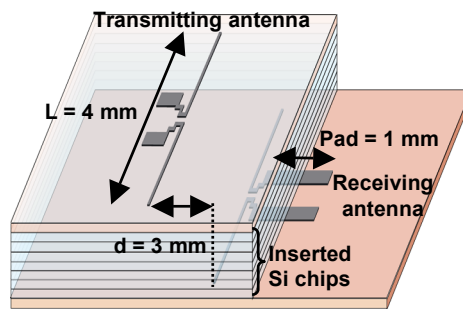Fig. 4. Measurement set-up for UWB signal transmission characteristics in time domain.

Fig. 5. Measurement sample for signal transmission through stacked Si chips (antenna length (L) = 4 mm, horizontal separated distance (d) = 3 mm, and pad length = 1 mm).
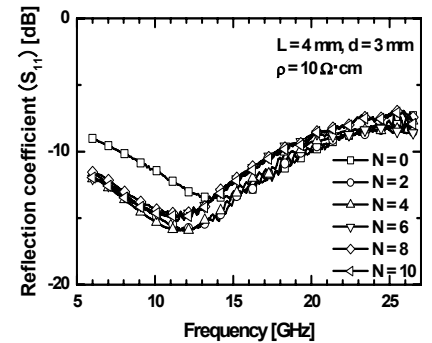
Fig. 6. Influence of the number of inserted Si chips on reflection coefficient when frequency range changed from 6 to 26.5 GHz.
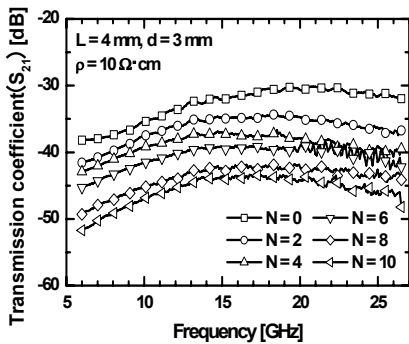
Fig. 7. Influence of the number of inserted Si chips on transmission coefficient when frequency range changed from 6 to 26.5 GHz.
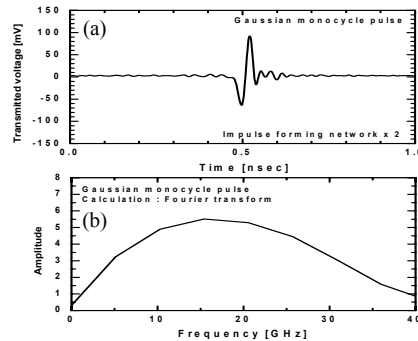
Fig. 8. (a) Transmitted Gaussian monocycle pulse, (b) frequency spectrum of transmitted Gaussian monocycle pulse.
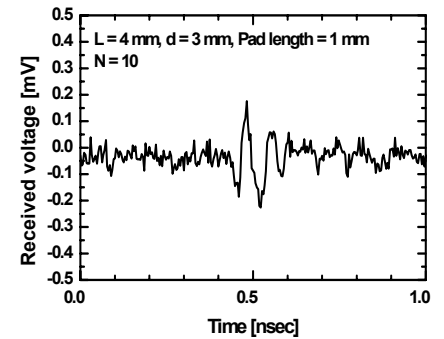
Fig. 9. Received Gaussian monocycle pulse through 10 stacked Si chips.
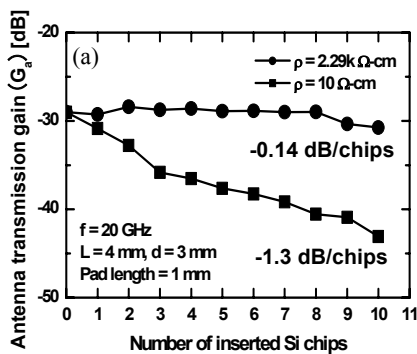
Fig. 10. Dependence of the number of inserted Si chips with resistivity of 10 and 2290 Ω·cm (a) antenna transmission gain at 20 GHz frequency, (b) received Gaussian monocycle pulse peak-to-peak voltage.
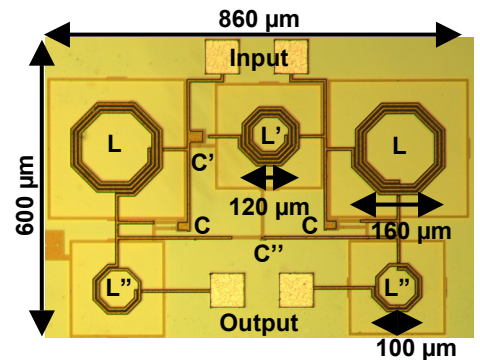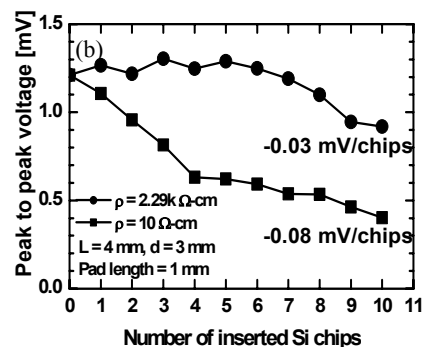
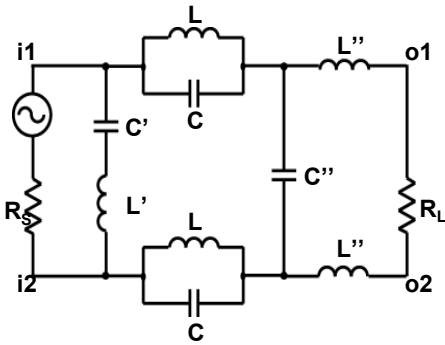Fig. 11. Chip photograph of integrated notch filter fabricated by use of 0.18-μm CMOS technology.

Fig. 12. Equivalent circuit of notch filter (L=4.9 nH, C=159 fF, L'=1.68 nH, C'=517 fF, L"=0.7 nH, C"=517 fF, and R_S=R_L=100 Ω).
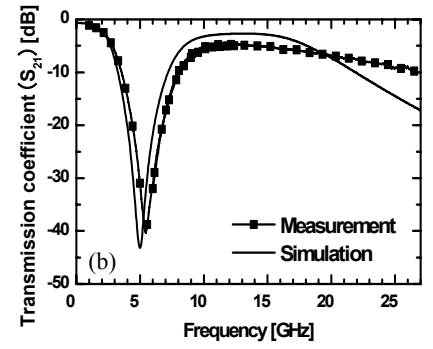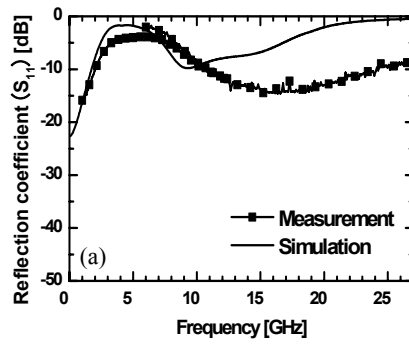

Fig. 13. Measured and simulated results of integrated notch filter (a) reflection coefficient (S_{11}), (b) transmission coefficient (S_{21}).
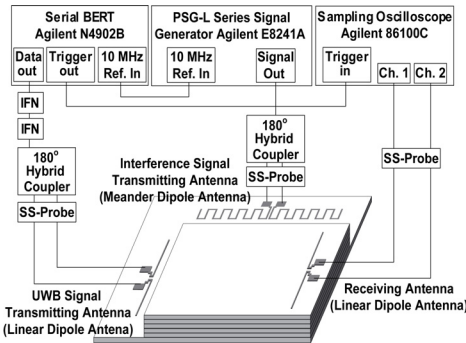

Fig. 14. Measurement set-up for UWB signal transmission with interference of sinusoidal wave using on-chip Si integrated antennas.
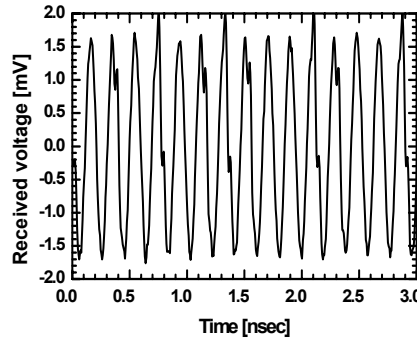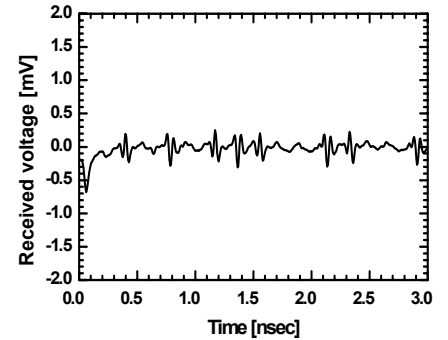

Fig. 15. Received UWB pulse trains with interference of 5.2 GHz sinusoidal wave.

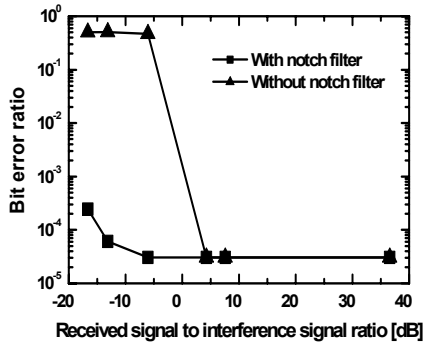Fig. 16. Received UWB pulse trains through integrated notch filter.

Fig. 17. Bit error rate versus received signal to interference signal ratio with and without integrated notch filter.
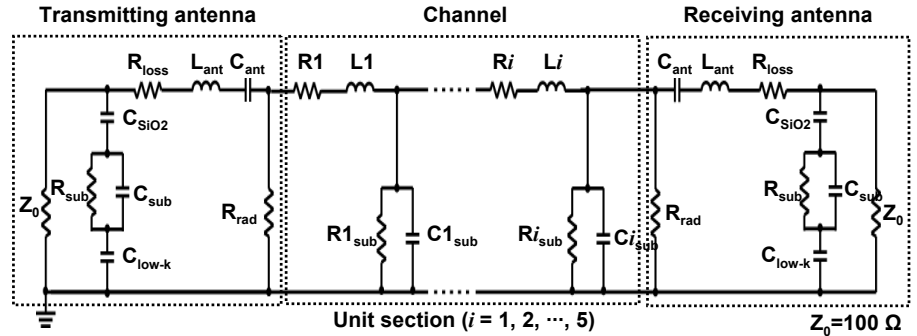

Fig. 18. Equivalent circuit model of Si integrated antennas including signal propagation channel (Z_0: characteristic impedance).
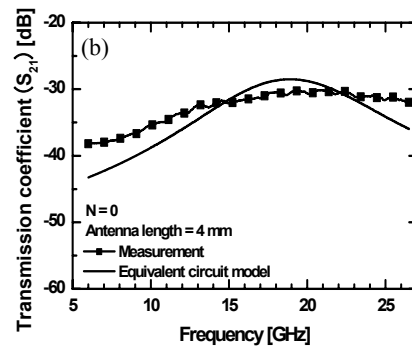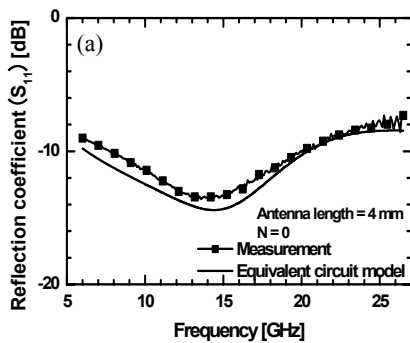

Fig. 19. Comparison of simulation using equivalent circuit model with measurement for stacked Si chip (a) reflection coefficient (S_{11}), (b) transmission coefficient (S_{21}).
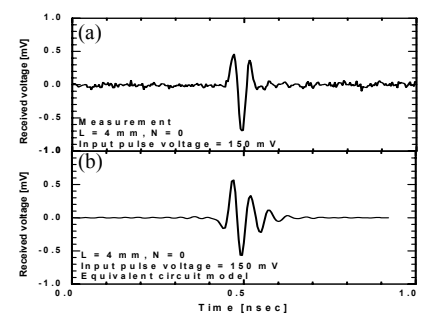

Fig. 20. Comparison of simulation using equivalent circuit model with measurement on received Gaussian monocycle pulse (a) measurement, (b) equivalent circuit model.