Workfunction Tuning of NiSi and Pd_2Si Fully-Silicided Gates by Predoping

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1. Introduction

Metal gates are expected to replace conventional poly-Si gate in order to eliminate a gate depletion and boron penetration. Since single metal with dual-workfunction is ideal for CMOS devices, workfunction tuning technique for several metals has been extensively investigated. Fully-silicided (FUSI) metal gate is one of the most promising candidates because of the relative ease of integration into conventional CMOS process. Furthermore, it is known that the workfunction of FUSI gates can be modulated by doping to poly-Si prior to silicidation [1-5]. In this paper, NiSi and Pd_2Si FUSI gate formation and workfunction tuning by predoping under various silicidation conditions were described.

2. NiSi FUSI Gates

Fabrication process flow of NiSi and Pd_2Si FUSI gate MOS diodes is shown in Fig. 1. In the case of NiSi FUSI gate, among various impurities [3, 4, 6], the maximum workfunction shift of -0.32 eV was obtained for 450°C silicidation with Sb-predoping (Fig. 2). However, no shift was obtained for 500°C. This difference originates from the Sb concentration at $NiSi/SiO_2$ interface as shown in Fig. 3, indicating that the workfunction shift is caused by the impurity pileup at the interface. On the other hand, the void formation at the oxide interface was observed for 450°C (Fig. 4). In addition, partial NiSi film peeling was found after unreacted Ni removal, as shown in Fig. 5. Such undesirable effects of predoping were found in the literature [3-9], which should be noted as a potential roadblock against practical use of NiSi FUSI gate.

3. Pd_2Si FUSI Gates

Three types of heating equipments, lamp heating in a sputtering chamber, hot-plate and RTA were used for silicidation. The major difference among them was heating ramp-up rate. Fig. 6 shows XTEM (cross-sectional TEM) image of Pd_2Si FUSI gate formed at 250°C with lamp heating. Needle-like silicide growth at the surface, void formation at the Pd_2Si/SiO_2 interface and a layered FUSI structure were observed. As illustrated in Fig. 7, these defects formation may be due to locally enhanced Si upward diffusion, which could be induced by silicidation at lower temperature during ramp-up. In the case of hot-plate heating, only the Pd_2Si phase was formed, which was confirmed by X-ray diffraction [10]. This is attributed to higher ramp-up rate because of large thermal capacity ratio of the hot-plate and a Si substrate. However, the voids at the interface were still formed at 250°C even with the hot-plate heating especially for the predoped case, as shown in Fig. 8. This void formation was avoided by raising the silicidation temperature to 300°C for P and Sb, but not for As. These results indicate that the ramp-up rate for silicidation annealing as well as the silicidation temperature and the presence of impurities are key factors to control the silicide formation.

The workfunction of undoped Pd_2Si FUSI gate was estimated to be 4.57 eV. Fig. 9 shows C-V characteristics for undoped and P-, As-, and Sb-predoped Pd_2Si FUSI gate MOS diodes. The positive flatband voltage (V_{FB}) shifts were obtained in spite of n-type dopants. The maximum V_{FB} shift obtained with P was +0.25 V regardless of the implantation dose. No interfacial layer formation was found in the XTEM image as shown in Fig. 10. From EDX analysis, P signal was detected only in the Pd_2Si layer in the vicinity of the Pd_2Si/SiO_2 interface. These results indicate that impurity pileup at the interface is an origin of the workfunction shift, as in the case of NiSi. On the other hand, the V_{FB} shift of -0.30 V was obtained with BF_2, as shown in Fig. 11. Furthermore, the V_{FB} shift of +0.30 V was obtained with F, despite no shift in NiSi [3, 4]. It is interesting that the Pd_2Si FUSI gate workfunction shifts by As-, P-, Sb- and BF_2-predoping are all in the opposite direction to the NiSi [1-4, 6-8] and PtSi [11] FUSI cases.

4. Conclusion

FUSI gate formation and workfunction tuning of NiSi and Pd_2Si has been investigated. Side effect of predoping, such as void formation at the oxide interface, is a common issue for the FUSI gate formation. The Pd_2Si FUSI gate workfunction shifts with various impurities are all in the opposite direction to the NiSi FUSI case.

Acknowledgement

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- p-Si(100)
- LOCOS formation
- Gate oxidation (5,10nm)
- poly-Si deposition (NiSi:100nm, Pd_2Si:60nm)
- ***Impurity ion implantation***
- ***Metal deposition (Ni:60nm, Pd:100nm)***
- ***Full-silicidation***
  - ***NiSi : 450°C 25min, 500°C 5min***
  - ***Pd_2Si : 250°C, 300°C 5min***
- Unreacted metal removal (Wet etch)
- Post metallization annealing (400°C, 30min)

Fig. 1 Fabrication process flow of NiSi and Pd_2Si FUSI gate MOS diodes.

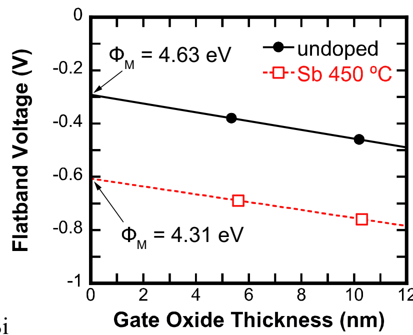


Fig. 2 Flatband voltage extracted from the C-V characteristics as a function of gate oxide thickness for undoped and Sb-doped NiSi FUSI gate MOS diodes.

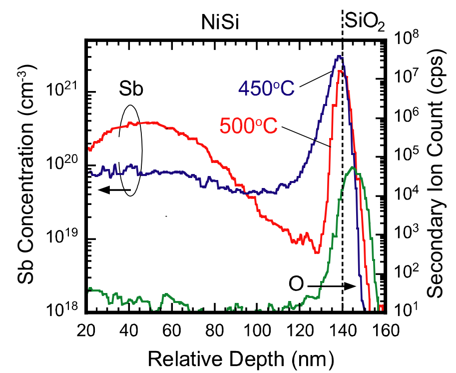


Fig. 3 Sb depth profiles in NiSi FUSI gate MOS structures formed at 450 and 500°C .

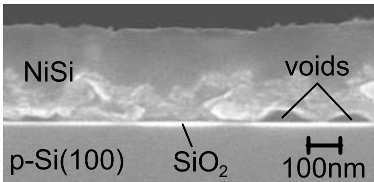
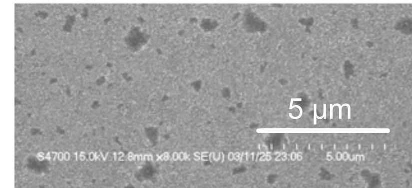


Fig. 4 Cross-sectional SEM image of Sb-doped NiSi FUSI gate MOS structure formed at 450°C .

Fig. 5 Plan-view SEM image of Sb-doped NiSi FUSI gate MOS structure formed at 450°C. Partial NiSi peeling off was found after unreacted Ni removal process.



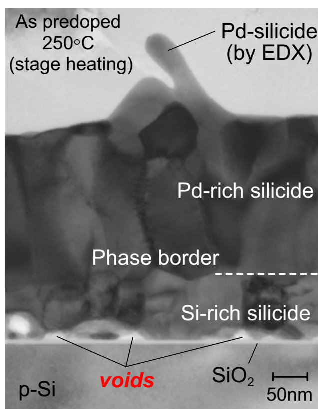


Fig. 6 XTEM (cross-sectional TEM) image of As predoped Pd_2Si FUSI gate formed at 250 °C with lamp heating in a sputtering chamber. Initial Pd and poly-Si thicknesses were 180nm and 100nm, respectively. Too slow ramp-up rate was not suitable for forming a uniform single phase film.

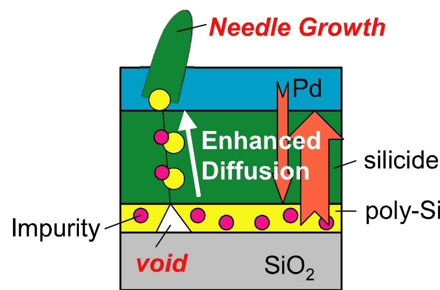


Fig. 7 Schematic illustration of defect formation mechanism during silicidation reaction. Locally enhanced Si diffusion toward the surface would result in void formation at the oxide interface and the needlelike silicide growth.

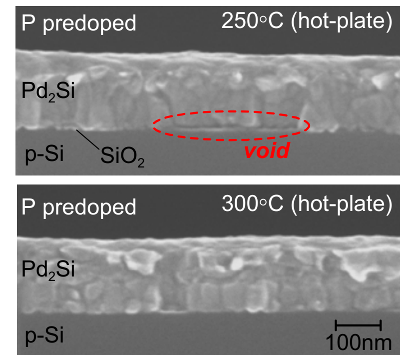


Fig. 8 Cross-sectional SEM images of Pd_2Si FUSI gate formed at 250 and 300°C with hot-plate heating. Needle growth was not found, but the void was formed at the oxide interface for 250°C silicidation.

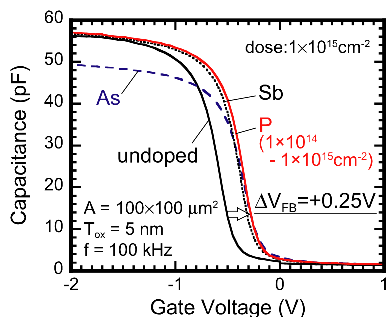


Fig. 9 C-V characteritstics of As-, P-, and Sb-predoped FUSI Pd_2Si FUSI gate MOS diodes. V_{FB} shift of +0.25 V was obtained with P-predoping regardless of implanted dose. Capacitance reduction occurred with As-predoping.

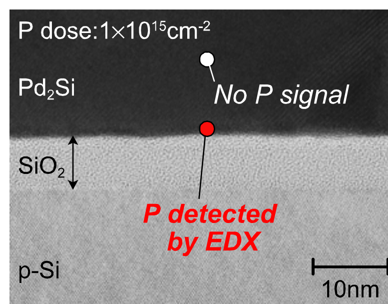


Fig. 10 XTEM image of the interfaces in P predoped Pd_2Si FUSI gate MOS diode. P signal was detected at the Pd_2Si/SiO_2 interface by EDX analysis.

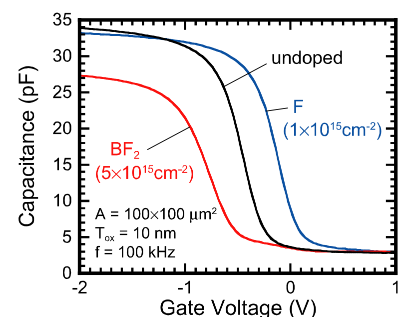


Fig. 11 C-V characteritstics of BF_2- and F-predoped FUSI Pd_2Si FUSI gate MOS diodes. V_{FB} shift of -0.3 V and +0.3V were obtained with BF_2 and F, respectively.