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Workfunction Tuning of NiSi and Pd_2Si Fully-Silicided Gates by Predoping

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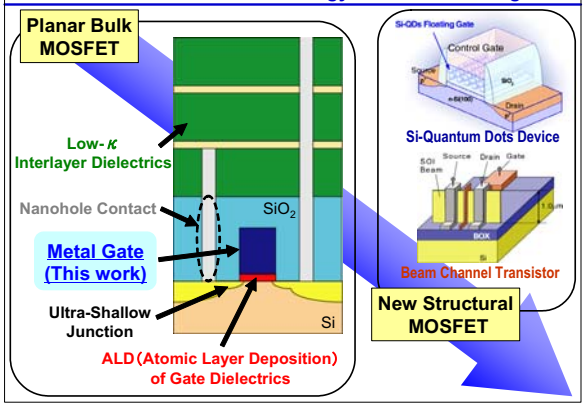
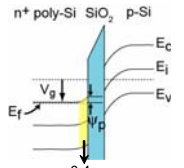
Fundamental Device Technology in 21st COE Program

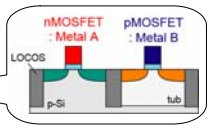


Why Metal Gate ?

Downscaling of gate oxide thickness → MOSFET technology development

- poly-Si gate (conventional)
  - Issue : Gate depletion effect
  - → Equivalent oxide thickness (EOT) increase
- Metal gate
  - Task : Dual-workfunction for CMOS
    - nMOS : low Φ_M (~4.05 eV)
    - pMOS : high Φ_M (~5.17 eV)
  - ■ Dual-metal gate structure
    - Complicated fabrication process





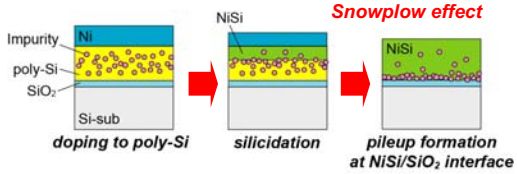
Single-Metal Tunable-Workfunction Gate Technology

NiSi Fully-Silicided (FUSI) Gate

■ ***NiSi workfunction can be tuned by impurity doping***

W.P.Maszara *et al.*, IEDM2002
J.Kedzierski *et al.*, IEDM2002

Snowplow effect

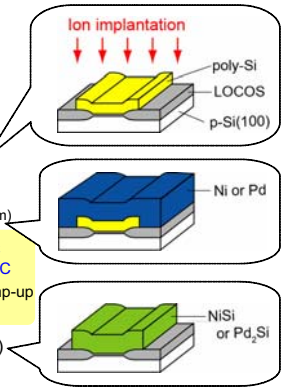


Issues: - insufficient for CMOS ($\Delta\Phi_M$= ~0.7eV)
- sensitive to process difference
- details of workfunction tuning mechanism ?

Exploring other materials ➡ ***Pd_2Si FUSI***

Fabrication Flow of NiSi & Pd_2Si FUSI gate MOS Diodes

- p-Si(100)
- LOCOS isolation
- Gate oxidation (5, 10nm)
- poly-Si deposition (NiSi:100nm, Pd_2Si:60nm)
- Gate patterning
- Gate doping: Ion Implantation
- Pre-annealing (900°C, 1min)
- Metal deposition (Ni:60nm, Pd:100nm)
- Full Silicidation { NiSi: 450, 500°C; Pd_2Si: 250, 300°C
  - Sputtering stage heating: slow ramp-up
  - Hot-plate, RTA: fast ramp-up
- Unreacted Pd removal (wet etch)
- PMA (400°C 30min, in 20%H_2)

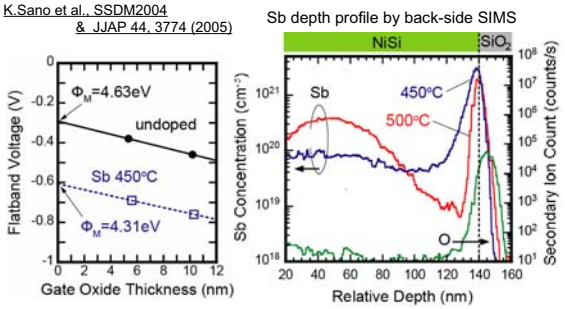


NiSi

Workfunction Tuning of Sb Predoped NiSi FUSI

K.Sano et al., SSDM2004 & JJAP 44, 3774 (2005)

Sb depth profile by back-side SIMS



450°C : $\Delta\Phi_M$ = -0.32eV
500°C : no Φ_M shift

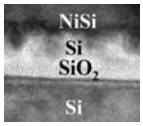
Pileup peak concentration : 450°C > 500°C

Adverse Effects of Predoping

■ *Remaining amorphous Si*

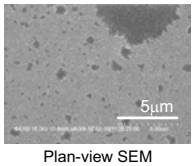
As doped

D. Aimé *et al.*, IEDM2004

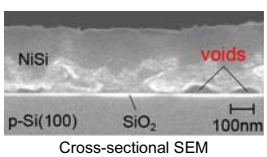


■ *NiSi peeling off and void formation at NiSi/SiO_2 interface*

Sb doped K.Sano et al., SSDM2004 & JJAP 44, 3774 (2005)



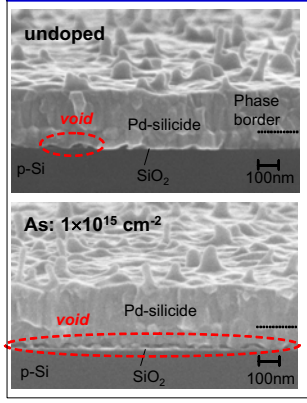
Plan-view SEM



Cross-sectional SEM

Pd_2Si

Defect Formation in Pd_2Si (Stage Heating)



250°C, 5min (Stage heating)

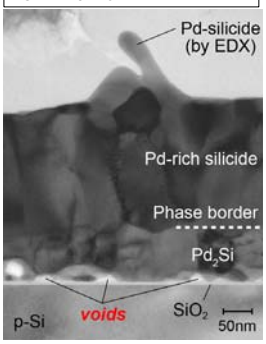
Silicidation is completed, but…

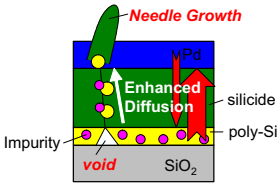
- Mixed silicide phases
- Needle-like structures on surface
- Void formation at oxide interface

Doping leads to an increase in void density

Issue of Sputtering Stage Heating

250°C, 5min (Stage heating)
As: 1×10^{15} cm^{-2}



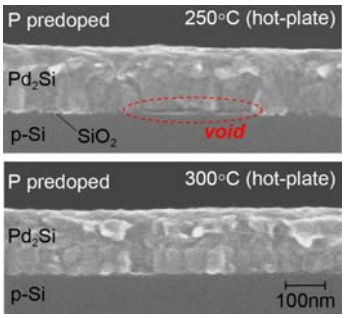


Stage heating:
Slow ramp-up (1°C/s)

Silicidation reaction at low temperature

Faster Ramp-up: Hot Plate

Silicidation Temperature Dependence

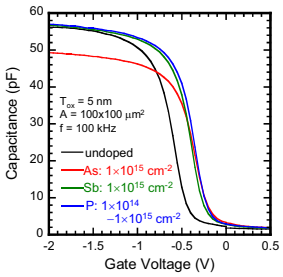


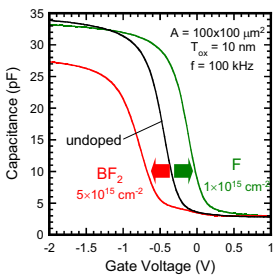
Voids are still observed for the doped sample

Void formation can be avoided at 300°C

Similar results were obtained with RTA (15°C/s).

Workfunction Tuning of Pd_2Si FUSI

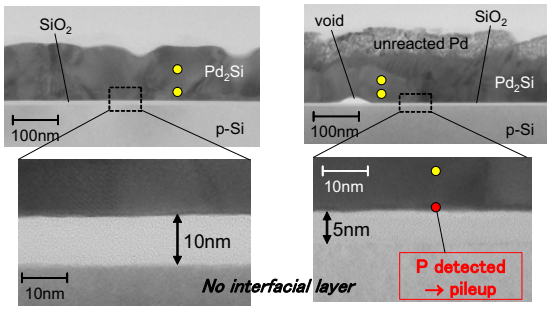




- range of the shift (~0.6 eV) is comparable to Ni-FUSI
- shift in opposite direction to Ni-FUSI & Pt-FUSI

XTEM of Pd_2Si/SiO_2 Interfaces

Undoped ●● EDX point P-doped (5×10^{15} cm^{-2})



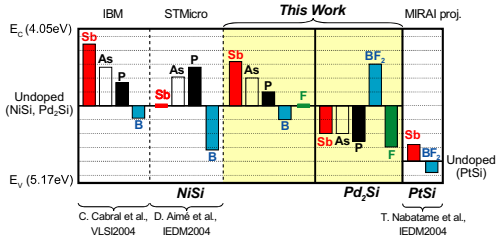
⇒ ***Workfunction shift by Impurity pileup***

Conclusion

- Void formation at FUSI/oxide interface depends on silicidation temperature & predoping condition

  Common issue for FUSI gate formation

- Workfunction tuning of NiSi & Pd_2Si FUSI gates



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